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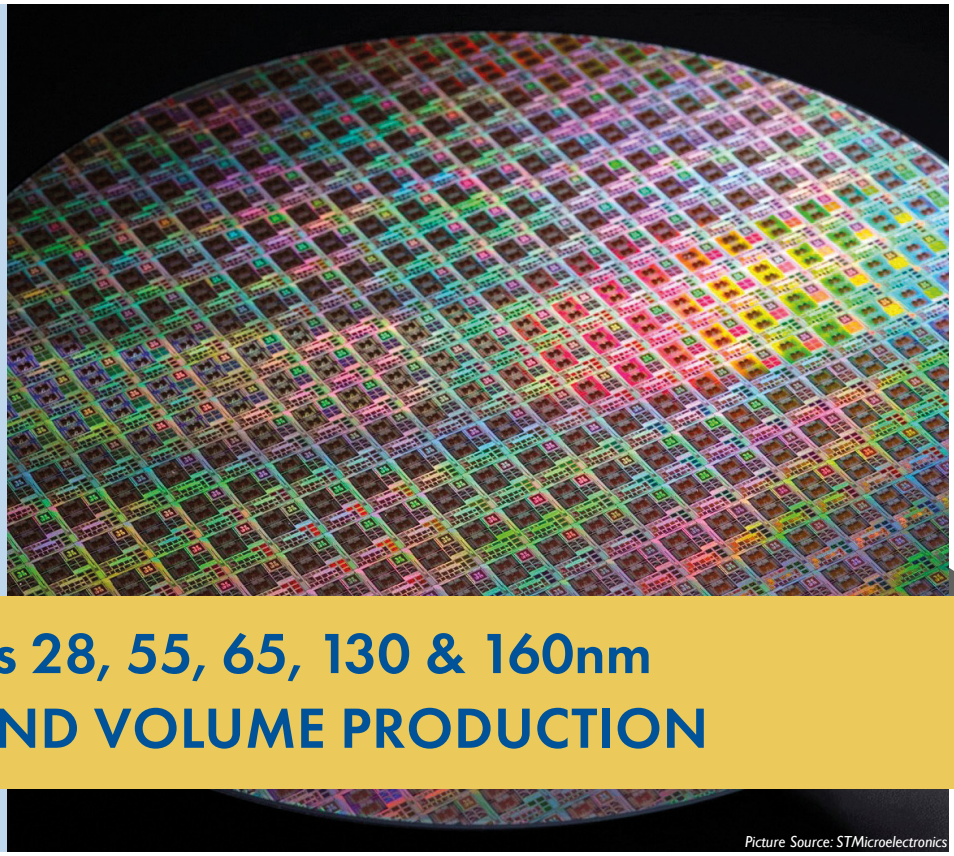

Picture Source: STMicroelectronics

# STMicroelectronics 28, 55, 65, 130 & 160nm PROTOTYPING AND VOLUME PRODUCTION

**EUROPRACTICE provides access to STMicroelectronics CMOS, BiCMOS SiGe and High Voltage Technologies for Multi-Project-Wafer Prototyping and Small Volume Production.**

## Why EUROPRACTICE?

- Affordable and easy access to Prototyping and Small Volume Production services for academia and industry.
- MPW (Multi-Project-Wafer) runs for various technologies, including ASICs, Photonics, MEMS and more.
- Advanced packaging, system integration solutions and test services.

## Why STMicroelectronics?

- Leading European foundry for analog/mixed-signal (MS) semiconductor applications.
- Technologies ranging from 160nm to 28nm MS CMOS, FDSOI, SiGe, SOI, HV for telecommunication, automotive, industrial and other applications.
- Best-in-class high performance processes at affordable prices. Extensive design-kits and libraries offer.

## Technology Highlights

### 28FDSOI & P28 – 28nm CMOS FDSOI + PCM NVM

The 28nm FDSOI CMOS technology is the most advanced node offered by STMicroelectronics. SOI based technology provides low leakage devices and wide back biasing voltage capabilities. Main applications are for low power digital and mixed-signal (MS)/RF applications. Extensive design kit and libraries are offered with compatibility with a wide range of CAD tools.

The new P28 technology is directly derived from the 28FDSOI one and integrates a non-volatile phase change memory to address automotive MCUs, Grade0 applications. It comes with a renewed IP offer combining large performance and design flexibility, with all the advantages of the FDSOI platform (power and energy efficiency, analog performance for MS and RF design, and robustness for mission critical applications).

### B55X – 55nm SiGe BiCMOS

The B55X technology takes over from the B55 one while drastically improving its performance. This new technology manages to combine higher gain and speed of bipolar transistors (the cut-off frequency is for exemple improved from 320 to 400 GHz) with even lower consumption of MOS transistors, aligned with that of the equivalent CMOS platform. It further facilitates the integration of RF, analog and digital parts on a single chip, and definitely remains the European flagship industrial BiCMOS technology for RF applications.

### C65LPGP – 65nm LP&GP CMOS

Standard CMOS process with digital, mixed-signal and RF capabilities. RF components like inductors, varactors and MIM capacitors are provided. This is a technology of choice for applications where a high density of digital circuitry is required along with analog components, i.e. for mixed-signal applications.

## B9MW – 130nm SiGe BiCMOS

130nm SiGe process with Bipolar transistor and thick metal layers for RF/mmW applications (Frequencies up to 77 GHz), wireless communication (around 60GHz for WLAN) and optical communications systems.

## H9A – 130nm HV CMOS

Low Power 130nm CMOS process with the extension of the RRAM/OxRAM NVM done as a post-process at CEA-Leti.

## H9SOI-FEM – 130nm RFSOI CMOS

H9-SOI-FEM is built on the same solid basis of the previous standard H9SOI technology and shares with it the robustness, the capability to address all FEM (Front End Module) applications (RF Switches, PA, LNA) and the expertise in RF SOI process.

## BCD8sP & BCD8s-SOI – 160nm BCDMOS

Smart-Power BCD8sP and BCD8s-SOI technologies combine high power transistors with low power digital and analog devices on a single chip. This technology is dedicated to power management systems, power supplies, motor drivers, amplifiers.

## Technology Details

### 28FDSOI

- 28nm drawn poly length.
- Triple well. Fully Depleted SOI devices with ultrathin BOX and Ground Plane.
- Body biasing. Dual Vt MOS transistors (LVT, RVT).
- 8 metal layers for interconnect.
- 2 thick Cu top metal (0.88 micron).
- Dual gate oxide (1.0V for core and 1.8V for IO).
- Low k inter-level dielectric.
- Fringe MOM capacitors.
- Inductors Analog / RF capabilities
- Various power supplies supported: 1.8V, 1.0V.
- Standard cell libraries.
- Embedded memory (Single port RAM / ROM / Dual port RAM).

### P28

- 28nm drawn poly length.
- Triple gate oxide: 1V, 1.8V & 5V.
- High & standard Vt LP MOS transistors.
- Copper metallization with 11 levels (including 1 thick top metal) + NiPd finish.
- OTP, ROM, RAM + PCM.

PCM main features outlook:

- High density PCM cell (< 0.04 $\mu m^2$);
- Fast access time (< 15 ns);
- High endurance (1.5K write cycles – 1PPM);
- Long retention time (25 years – 1PPM).

### B55X

- 55nm drawn poly length
- Si/SiGe:C HBTs, natural NPN & PNP BJTs
- Ft > 400GHz & Fmax > 500GHz
- Deep NWell, optional DTI
- Double gate oxide: 1.2V (LP) & 2.5V (GP)
- High & standard Vt LP MOS transistors
- Natural active, poly & metal resistors
- Natural, MOM & MIM capacitors
- Copper metallization with 7 levels (including 2 thick top metals) + alucap
- Standard & IO cells (more to come)
- OTP available, ROM & RAM offer to be defined.

### C65LPGP

- 65nm drawn poly length.
- 7 metal layers.
- Deep Nwell and Deep Trench Isolation.
- Triple Vt MOS transistors (LVT, RVT and SVT).
- Low Power and General Purpose MOS transistors.
- Dual gate oxide (1.0V for core and 2.5V for IO).
- MIM & Fringe MOM capacitors.
- Inductors Analog / RF capabilities.
- Various power supplies supported: 2.5V, 1.2V, 1V.
- Standard cell libraries.
- Embedded memory (Single port RAM / ROM / Dual Port RAM).

### B9MW

- 130nm drawn, 130nm effective.
- Deep Nwell and Deep Trench Isolation.
- Double Vt transistor offering (Low Leakage, High Speed).
- Dual gate oxide (1.2V for core and 2.5V for IO).
- Bipolar SiGe transistors.
- Typical Ft (for 2 families above): 230/150GHz.
- Power supply 1.2V.
- 6 Cu metal layers.
- MIM capacitors.
- Standard cell libraries.
- Embedded memory (Single port RAM).

### H9A

- CMOS gate length: 130nm drawn poly length.
- Deep Nwell, Deep Trench Isolation.
- Vt transistor offering (Low Power, Analog).
- Bipolar NPN transistors.
- Typical beta: 90.
- Ft Max @ Vbc=0: 2,4GHz.
- 2 specific implant levels: NDRIFT & PDRIFT MIM 5fF/µm2.
- Double gate oxide for analog features.
- 4 metal layers in standard Fluorinated SiO2 (intermetal dielectric).
- Power supply: 1. 2V for Digital, 4.6V for Analog application multiple.
- Standard cell libraries.

### H9SOI-FEM

- CMOS gate length: 130nm.
- SOI wafers with high resistive substrate 2.5V.
- Body Contacted CMOS.
- Floating Body CMOS 5.0V NLD-MOS.
- PLDMOS 1.2V High Speed 130nm.
- 4 metal layers for interconnect
- Ultra-thick Cu top metal (4.0 micron).
- High Linearity MIM capacitor.
- Standard cell libraries.

### BCD8sP & BCD8s-SOI

- Bipolar-CMOS-DMOS.
- 4 Metal Levels with last Al Thick-Power metal.
- Baseline 3.3V CMOS.
- Medium Voltage Modules: 6V / 20V / 40V NDMOS and PDMOS.
- High Voltage Modules: 70V / 100V / 140V / 200V NDMOS and PDMOS Optional 2nd gate oxide for 1.8V.
- CMOS Dielectric Isolation on SOI.
- Available memory: OTP.



Would you like to discover more?

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