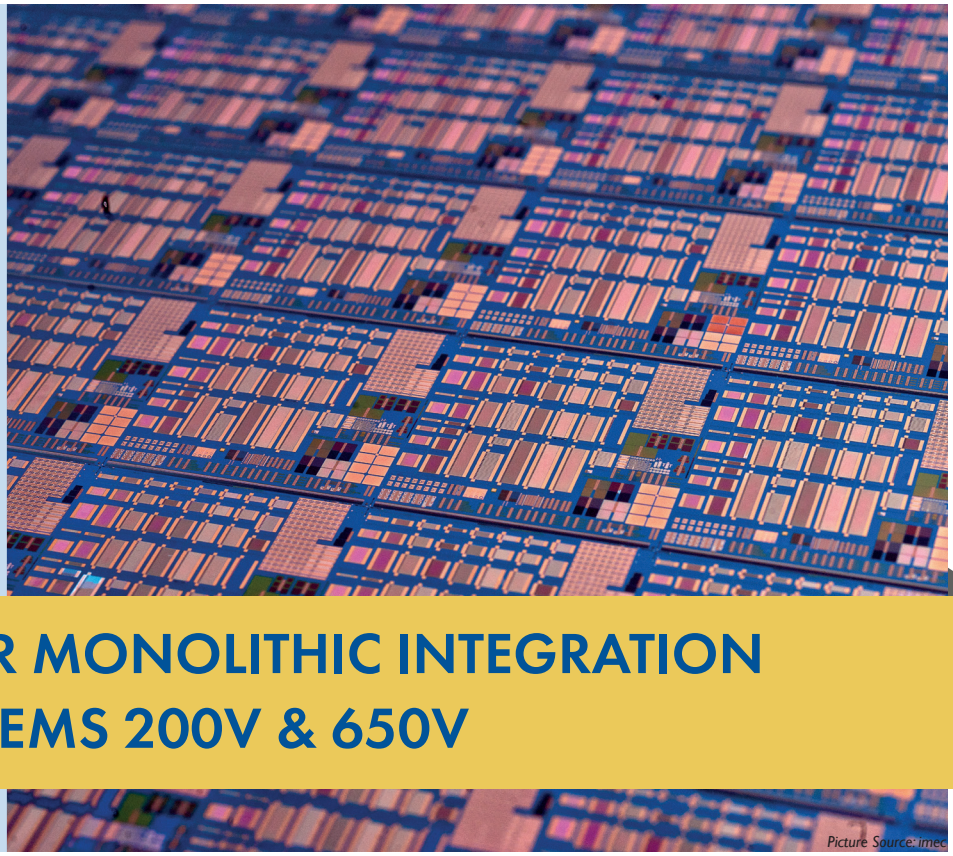


imec GaN-IC FOR MONOLITHIC INTEGRATION OF POWER SYSTEMS 200V & 650V

EUROPRACTICE offers Multi-Project-Wafer and Volume Production services of imec technologies, including GaN-IC for monolithic integration of power systems.

Why EUROPRACTICE?

- Affordable and easy access to Prototyping and Small Volume Production services for academia and industry.
- MPW (Multi-Project-Wafer) runs for various technologies, including ASICs, Photonics, MEMS and more.
- Advanced packaging, system integration solutions and test services.

Why imec GaN-IC?

- Integrating multiple transistors on a single IC using trench isolation.
- Reducing system parasitic inductance.
- Saving package cost by packaging one instead of multiple devices.
- Working with a world-leading research and innovation hub in nanoelectronics and digital technologies headquartered in Belgium.

Technology Highlights

To unlock the full potential of GaN power electronics, imec offers a unique GaN-on-SOI process. The deep-trench isolation implemented in this process provides full isolation between power devices, drivers, control and protection circuits. This, in turn, enables the manufacturing of complex GaN ICs. In addition to accommodating smaller form factors, the close proximity of devices drastically reduces parasitic inductance, resulting in a significant switching speed enhancement.

Imec's monolithic integration allows the cointegration of the driver, resulting in lower parasitic inductances, unlocking the full potential of the fast-switching speed of GaN power devices. Further functionality can be added through the low-voltage logic and analog switches, the high-ohmic and low-ohmic resistors and the integrated MIM-capacitors.

State-of-the-art e-Mode Power Devices on 200mm/8-inch Si Wafer

GaN based power devices, mainly available as discrete components, have pushed operating frequencies and efficiencies of Switch Mode Power Supplies (SMPS) to record levels. However, the technology's full potential can only be unlocked by reducing the parasitic inductances. Imec's GaN-on-SOI technology allows to monolithically integrate logic and power components onto the same die, minimizing parasitic inductance.

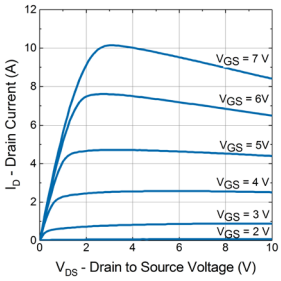
GaN-on-SOI Design Kit

To make this technology more easily available, imec provides an extensive GaN-on-SOI Process Design Kit (PDK), both for 200V and 650V technologies. These kits include process documentation, library devices, layout guidelines for custom design, verification, and models. Low-ohmic and high-ohmic resistors are provided, as well as Metal/Oxide/Metal capacitors and low voltage logic devices. These enable customers to design highly integrated GaN power systems on chip. The PDKs are available after signing imec's GaN-IC Design Kit License Agreement (DKLA).

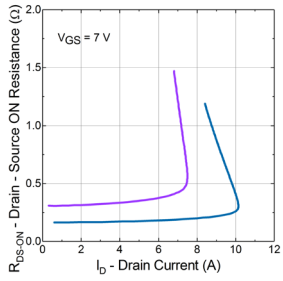
200 V e-MODE p-GaN HEMT

Datasheet Power Device with Weff = 36 mm

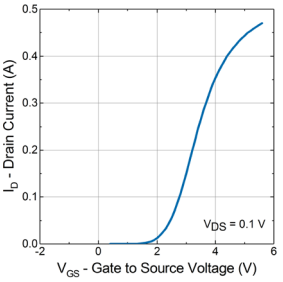
Symbol	Description	Test Conditions	MIN	TYP	MAX	UNIT
ABSOLUTE MAXIMUM RATINGS						
BV_{DS}	Drain-Source voltage			>200		V
I_D	Pulsed Drain current	1 ms pulse			10	A
V_{GS}	Gate-Source voltage				7	V
ON/OFF STATE CHARACTERISTICS						
BV_{DS}	Drain-Source voltage	V_{GS} = 0 V	200			V
I_{DSS}	Drain-Source leakage	V_{GS} = 0 V, V_{DS} = 200 V T=25°C		100	1000	nA/mm
		V_{GS} = 0 V, V_{DS} = 200 V T=150°C		50	500	µA/mm
I_{GSS}	Gate forward leakage	V_{DS} = 0 V, V_{GS} = 7 V T=25°C		20	100	µA/mm
R_{DS-ON}	Drain-Source ON resistance	V_{GS} = 7 V, V_{DS} = 0.1 V T=150°C		7	9	µA/mm
		V_{GS} = 7 V, V_{DS} = 0.1 V T=150°C		14	18	Ωmm
V_{TH}	Gate threshhold voltage	maximum g_m	2.1	2.5	2.9	V
DYNAMIC CHARACTERISTICS						
C_{ISS}	Input capacitance	V_{GS} = 0 V, V_{DS} = 200 V, f = 1 MHz		55		pF
C_{OSS}	Output capacitance			35		pF
C_{RSS}	Reverse transfer capacitance			0.97		pF



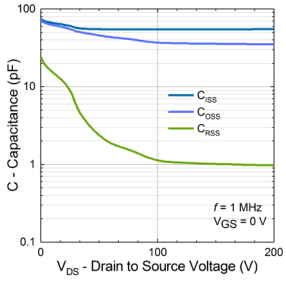
Typical IDS vs.VDS curve at T=25 °C



RDS vs. VDS(on) vs IDS at T=25 and 150 °C



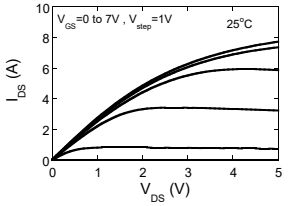
Typical IDS vs.VGS curve at T=25 °C



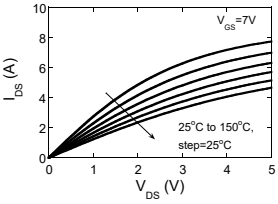
Typical CISS , COSS and CRSS vs VDS at T=25 °C Measurements on-wafer (no packaging parasitics included).

650 V e-MODE p-GaN HEMT

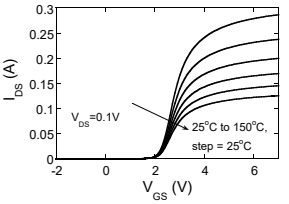
Symbol	Description	Test Conditions	MIN	TYP	MAX	UNIT
ABSOLUTE MAXIMUM RATINGS						
BV_{DS}	Drain-Source voltage			>650		V
I_D	Pulsed Drain current	1 ms pulse			7.5	A
V_{GS}	Gate-Source voltage				7	V
ON/OFF STATE CHARACTERISTICS						
BV_{DS}	Drain-Source voltage	V_{GS} = 0 V	650			V
I_{DSS}	Drain-Source leakage	V_{GS} = 0 V, V_{DS} = 650 V T=25°C		100	1000	nA/mm
		V_{GS} = 0 V, V_{DS} = 650 V T=150°C		50	500	µA/mm
I_{GSS}	Gate forward leakage	V_{DS} = 0 V, V_{GS} = 7 V T=25°C		20	100	µA/mm
R_{DS-ON}	Drain-Source ON resistance	V_{GS} = 7 V, V_{DS} = 0.1 V T=25°C		14	18	µA/mm
		V_{GS} = 7 V, V_{DS} = 0.1 V T=150°C		30	35	Ωmm
V_{TH}	Gate threshhold voltage	maximum g_m	2.1	2.5	2.9	V
DYNAMIC CHARACTERISTICS						
C_{ISS}	Input capacitance	V_{GS} = 0 V, V_{DS} = 650 V, f = 1 MHz		47.2		pF
C_{OSS}	Output capacitance			14.6		pF
C_{RSS}	Reverse transfer capacitance			0.12		pF



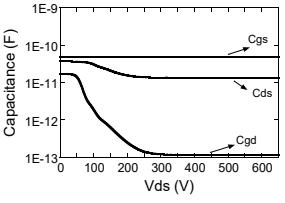
Typical IDS vs. VDS curve at T=25 °C



Temperature dependence of IDS vs.VDS curve at VGS=7V



Temperature dependence of IDS vs VGS curve at VDS=0.1V



Typical CGS, CDS and CGD vs VDS at T=25 °C. Measurements on-wafer (no packaging parasitics included)

Would you like to discover more?

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