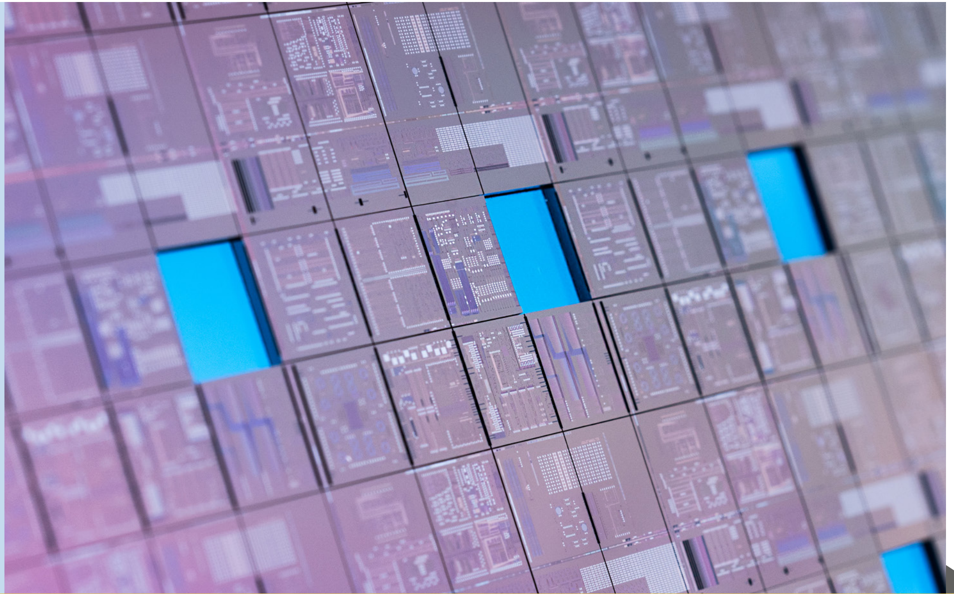


Picture Source: imec

imec Si-PHOTONICS PLATFORM PROTOTYPING AND VOLUME PRODUCTION

EUROPRACTICE provides Multi-Project-Wafer prototyping and Volume Production services of imec Silicon Photonics ISiPP50G and Passives+.

Why EUROPRACTICE?

- Affordable and easy access to Prototyping and Small Volume Production services for academia and industry.
- MPW (Multi-Project-Wafer) runs for various technologies, including ASICs, Photonics, MEMS and more.
- Advanced packaging, system integration solutions and test services.

Why imec Photonics?

- Cost-effective, highly reproducible and CMOS compatible fabrication.
- Regularly scheduled MPW runs and dedicated mask runs.
- Complete PDKs including technology details, design and layout rules, and a library of building block components.
- World-leading research and innovation hub in nanoelectronics and digital technologies headquartered in Belgium.

Technology Highlights

Si-Photonics ISiPP50G

The platform enables cost-effective silicon photonic ICs for:

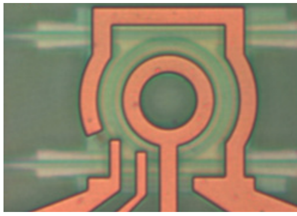
- High-performance optical transceivers (50Gb/s and beyond) for datacom, telecom and access networks
- Optical sensing (gas, pressure, strain) and read-out ICs
- Biomolecule detection, drug development, point-of-care diagnostics

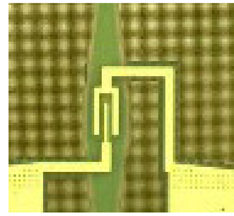
The ISiPP50G platform co-integrates a wide variety of passive and active components to support a wide range of optical transceiver architectures at data rates of 25Gb/s or 50Gb/s. The offered integrated components include low-loss waveguides with an option to expose them to the ambient, efficient vertical grating or broadband edge couplers, high-speed silicon electro-optic modulators, high-speed silicon-germanium electro-absorption modulators and high-speed germanium waveguide photo-detectors. iSiPP50G offers state-of-the-art performance, design flexibility and superior CD and thickness control. It is a fixed process technology (130nm) with a validated device library.

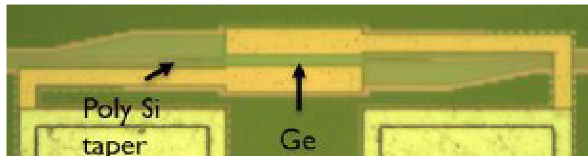
Si-Photonics Passives+

imec Si-Photonics Passives+ technology is a subset of iSiPP50G technology. The SOI layer can be etched at three different depths to enable integration of different photonic functions. A patterned poly-Silicon layer improves the performance of grating couplers for out-of-plane coupling to fibers and a deep etched trench at an edge of the chips, combined with edge-coupler components, provides optical access, with a broader optical bandwidth. In addition, a layer for metal-based heaters enables thermal tuning of the optical functions. Electrical access to the metal heaters is established through two additional levels of metal interconnect.

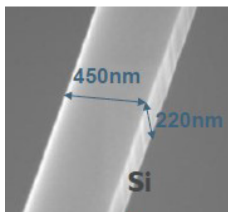
Active & Passive components based on ISIPP50G


Ring modulator


Germanium Photodetector



Electro Absorption Modulator

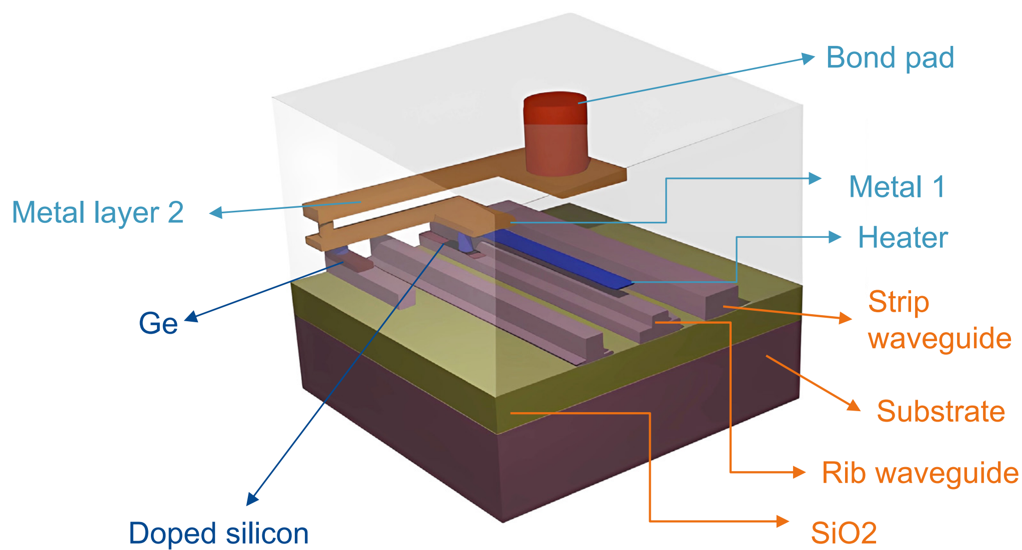


Low loss passive waveguide

Edge Coupler

Technology Details

Modules	Description	Enabled devices
3silicon patterning steps	3 etch depths in 220nm Si: 70nm, 150nm; 220nm (193 nm litho)	Strip/rib waveguides, various passive optical devices, silicon taper
Gate oxide and Poly-Silicon layer	1 etch depth: full poly etch (160nm) (193nm litho)	Advanced grating couplers, poly-Si waveguide
Metal-based heater	A layer for thermal tuning	Heaters
Two-level metal interconnect	Cu-based two-level metallization	Standard CMOS interconnects
Deep trench	Deep trench to expose edge coupler facets	Edge couplers
Ion implantation in Si	8 implants levels: 4x n-type and 4x p-type	Si carrier depletion, injection and accumulation devices, Ge Photodectors, doped Si resistors, …
Ge module	100% Ge(Si) RPCVD selective epitaxial growth & 2x implants levels	Ge Photodectors Ge(Si) EA modulator
Silicide tungsten contact module	Ohmic contacts to doped silicon	Standard CMOS contacts plugs
Aluminium passivation	Aluminium finish metallization	Standard CMOS interconnects



Si-Photonics ISIPP50G platform

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Would you like to discover more?

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