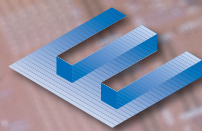# ACTIVITY REPORT
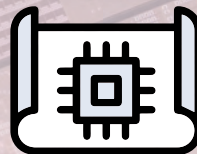## 2023-2024

EUROPRACTICE

EUROPRACTICE

The access point for electronic circuits and systems
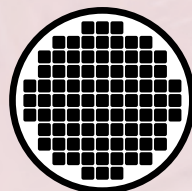
2023 at a glance

813
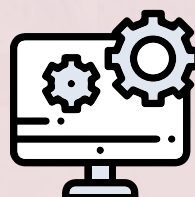submitted designs

30
training courses

48
webinars on youtube

20
foundries in the technology portfolio

16
design tool vendors

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FOREWORD

Dear customers, colleagues and friends,

Looking back at 2023, we can happily admit that EUROPRACTICE services had a successful year.

Indeed, the number of designs submitted for fabrication reached **813** exceeding the figures of 2022 by more than 10 %. Similar to previous years, the majority of these designs were manufactured by TSMC, a leading foundry in the global industry. Notably, the second place is occupied by a European R&D fab IHP, surpassing GlobalFoundries. Moreover, our technology portfolio has extended and now includes fabrication services of 20 foundries. Two of them joined us last year: Pragmatic with their flexible electronics (FlexIC) offer and UMS with GaN and GaAs technologies.

Together with MPW fabrication, other services in the EUROPRACTICE portfolio also showed very good results at the end of 2023. For instance, over the past year, we organised 40 training courses on design flows and different technologies, alongside eight webinars introducing participants to Pragmatic's FlexIC technology, compound semiconductors, and various aspects of IC design. Last but not least, our EUROPRACTICE community on social media has grown to nearly 3,500 followers on LinkedIn and 1,400 subscribers on YouTube, with almost 70,000 views.

2023 marked a significant year for the European microelectronics sector with the signing of the European Chips Act, emphasizing its strategic importance. At EUROPRACTICE, we remain committed to contributing to the growth of the semiconductor market in Europe by lowering barriers for our users to design and fabricate microelectronic devices and improve their skills in this domain.

In 2024, we continue to enlarge and diversify our offer by adding new technologies and services to our portfolio. We are currently working on establishing a design IP exchange repository, providing chiplet and system integration possibilities, and increasing support to startups and SMEs.

We are delighted that our efforts have been supported by Chips Joint Undertaking (Chips JU) through a funded project RETICLES: Research, Entrepreneurship, Training, IP-exchange & Chip pLatform of EUROPRACTICE Services. This support will enable us to continue maintaining and extending the EUROPRACTICE platform until September 2025.

We express our gratitude to all of you – our academic and industrial customers, as well as our technology and design tool suppliers – for your continued support of our services. Wishing you all a productive and successful 2024.

Looking forward to supporting your innovative projects and creating more success stories together,
Your EUROPRACTICE team at imec, UKRI-STFC, Fraunhofer IIS, CIME-P and Tyndall

TABLE OF CONTENTS

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EUROPRACTICE SERVICES

THE ACCESS POINT FOR ELECTRONIC CIRCUITS AND SYSTEMS

EUROPRACTICE offers a platform with a full range of services to design and fabricate microelectronic circuits and systems. For nearly 30 years, we have supported our customers in all critical steps from prototype design to volume production.

FABRICATION SERVICES
Cost-effective fabrication in technologies of leading foundries for both industrial and academic customers

DESIGN TOOLS
Affordable access to industry-standard design tools for European academia and its spinoffs

TRAINING & WEBINARS
In-depth hands-on training courses on design flows and technologies and free webinar series

EUROPRACTICE acts as a one-stop shop representing the prime interface between the academic and industrial customers on the one hand, and the technology providers on the other. Our suppliers include design-tool and IP-library vendors, foundries, assembly and test houses – who all provide state-of-the-art industry-grade technologies.
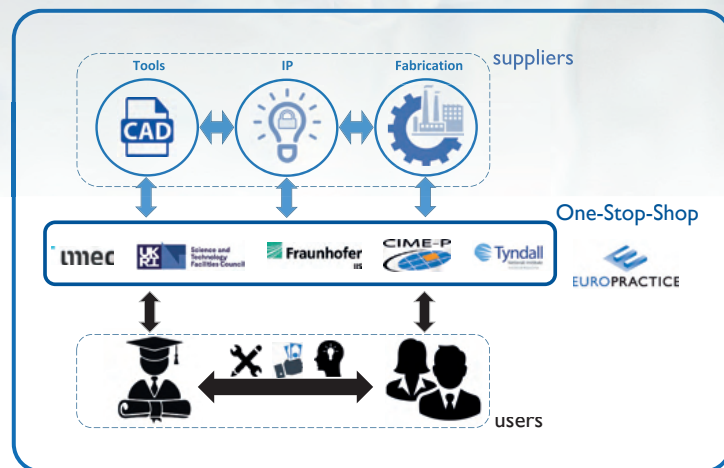
Thanks to this coordinated brokerage service, the EUROPRACTICE platform nurtures the growth of a microelectronic design ecosystem in Europe supporting industry and academia who look for affordable and easier access to electronic smart systems technologies. The barrier for users to access these technologies and services has been lowered by affordable pricing negotiated with vendors and, most importantly, by extensive customer support, stimulation and training.

As a result, EUROPRACTICE has served as a pan-European chip infrastructure for design innovation, used by more than 600 European academic and research institutions and 300 European SMEs. The service builds on the many years of experience of five consortium partners: imec, UKRI-STFC, Fraunhofer IIS, CIME-P, and Tyndall.

EXTENDING THE EUROPRACTICE PLATFORM

EUROPRACTICE was launched with the support of the European Commission in 1995 as a successor to EUROCHIP (1989-1995) to enhance European industrial competitiveness in the global market. Over the years, the platform has significantly evolved, introducing new services and technologies.

RETICLES

In 2022 – 2025, Chips Joint Undertaking (Chips JU) has been supporting EUROPRACTICE through a funded project RETICLES: Research, Entrepreneurship, Training, IP-exchange & Chip pLatform of EUROPRACTICE Services. This project will nurture the further growth of the design ecosystem in Europe, building on the existing EUROPRACTICE platform and further extending our offer. Here are some highlights:

MORE SUPPORT FOR STARTUPS AND SMES IN EUROPE

To support the semiconductor industry in Europe and create a breeding ground for deep-tech startups, EUROPRACTICE provides a large scope of services to European SMEs:

- ✓ Prototyping in a wide range of technologies in multiple foundries.
- ✓ Route to upscale to volume production with a full package of required services, including test, characterization and qualification.
- ✓ Tailored training courses to meet the specific needs of individual companies.
- ✓ Affordable access to design tools for academic spinoffs.
- ✓ Support of the subsequent commercialisation of academic research.

DESIGN IP EXCHANGE REPOSITORY

EUROPRACTICE will enhance design efficiency through design reuse and establishing IP exchange repositories. Through these repositories, users will be able to share their IP and access the IP provided by other users. The first repository for exchanging microelectronic design IPs has already been established in collaboration with CERN.

CHIPLETS & SYSTEM INTEGRATION

The creation of smarter integrated systems will be stimulated through advanced system integration of dissimilar semiconductor technologies and chiplets. In 2023 we successfully created a chiplet demonstrator to showcase the possibilities and advantages of heterogeneous integration of III-V materials onto silicon (see Figure 1).

In 2024 we will expand our System Integration portfolio by offering Micro Transfer Printing, a heterogenous integration technique where devices from one material system can be transferred from their native substrate material to a host substrate of a different material.

Fig. 1: Micro transfer printed lasers on silicon substrate.

AFFORDABLE ACCESS TO STATE-OF-THE-ART CAD TOOLS

EUROPRACTICE has negotiated lower prices with the major design tool vendors world-wide, as well as with IP and programmable device vendors. Consequently, European academic institutions can access EUROPRACTICE licenses of the most advanced EDA/CAD tools for a wide range of electronic system (including IC, MEMS, Photonics etc.) design at affordable prices for education and non-commercial research. The design tools are made available in vendor specific functional bundles that are cost effective, easy to install and are enhanced annually under maintenance contracts to add new functionality. In addition, the EUROPRACTICE service provides an infrastructure to allow its Members to access EDA/CAD vendor material, such as training material, on a scale which otherwise would not be possible.

The current EUROPRACTICE network of European academic institutions is the largest network in the world having a unique and uniform tool base for electronic system, IC, MEMS and Photonics design. Access to these advanced CAD tools allows our customers to participate in EC-funded projects, ranging from IP block and component design to the design of complete systems.

DESIGN TOOLS FOR ACADEMIC SPINOFFS

Spinoffs of European universities can access certain design tools at low cost via EUROPRACTICE in order to produce a proof-of-concept IC to demonstrate their IP/product. The resultant IP can then be fully commercialized for an additional agreed fee. The spinoff gains access to an industry-standard full IC design flow, suitable for all IC technologies.

EUROPRACTICE works flexibly with academic institutes and SMEs to facilitate effective innovation. For instance, we have mechanisms in place if an academic institute has developed a design using EUROPRACTICE tools and subsequently wishes to exploit this design commercially, either via a spin-out or by transferring the IP to an existing SME.

EASY ACCESS TO PROTOTYPING

It is challenging for small companies, academic and research institutions to obtain access to foundry fabrication lines since they often need a high level of technical support and require only a small-volume production for prototyping purposes. If they choose to work directly with a commercial foundry, the manufacturing costs will be very high.

This is when EUROPRACTICE comes into play. We help significantly reduce fabrication costs by opening access to Multi-Project-Wafer (MPW) runs and Multi-Level-Mask (MLM) services for prototyping and volume production respectively.

In addition, EUROPRACTICE offers a wide choice of technologies of world-leading foundries together with technical support and training.

TECHNOLOGY PORTFOLIO

The EUROPRACTICE portfolio includes a broad range of technologies, such as ASIC processes ranging from 0.35µm to 7nm, MEMS, Silicon and Glass Photonics, Compound Semiconductors, Microfluidics, and more. The ASIC processes have various options, including digital logic, RF, mixed-signal and high-voltage.

> **New technologies and foundries**
> In 2023, the EUROPRACTICE portfolio was further extended and included fabrication services of two more foundries. Our users can now access flexible electronics (FlexIC) of Pragmatic, and GaAs and GaN processes of United Monolithic Semiconductors (UMS). Soon, our offer will also include Graphene technologies of Graphenea.

Traditionally, EUROPRACTICE focuses on technologies from European-based companies as 17 of the 20 foundries have manufacturing facilities in Europe.

MULTI PROJECT WAFER AND MINI@SIC RUNS

By combining several designs from different customers onto the same mask set of a prototype run, known as Multi-Project-Wafer (MPW) run, the high cost of the mask set and the fabrication process is shared among the participating customers.

Fabrication of prototypes can therefore be as low as 5% to 10% of the cost of a wafer run for only one dedicated customer. A limited number of IC prototypes, typically 20-50, are delivered to the customer for evaluation, either as naked dies or as encapsulated devices. Only prototypes from fully qualified wafers are taken to ensure that the chips delivered will function "right first time". To achieve this, extensive Design Rule and Electrical Rule Checkings are performed on all designs submitted to the Service.

Since most of the designs fabricated for educational purposes are much smaller than the minimum block size on regular MPW runs, the concept of **mini@sic** was introduced in 2003. This solution allows to further lower prototype fabrication costs compared to standard MPW runs. The mini@sic principle is based on the following methodology: Several times per year, a foundry standard MPW block is bought and resold in smaller and cheaper sub-blocks or mini@sics. This program has been extended over the years and currently includes selected technologies from GlobalFoundries, IHP, TSMC, UMC and X-FAB.

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TECHNOLOGY PORTFOLIO 2024

ams OSRAM

ams 0.35µm CMOS C35B4C3

ams 0.35µm CMOS C35OPTO + BARC Diode option

ams 0.35µm HV CMOS H35B4D3

ams 0.35µm SiGe-BiCMOS S35

ams 0.18µm CMOS atC18c

em microelectronic

EM 110nm CMOS ALP011 logic

GlobalFoundries

GF SiGe 8XP

GF 130nm BCDlite-Gen2

GF 55nm BCDlite 55nm BCDlite

GF 45nm SPCLO Si-Photonics

GF 45RFE

GF 28nm SLPe

GF 22nm FDSOI

GF 12nm LP+

ihp

IHP SG25H5_EPIC (BiCMOS + Photonics)

IHP SG25 PIC (Photonics)

IHP SG13S 0.13µm SiGe:C

IHP SG13C 0.13µm SiGe:C

IHP SG13G2 0.13µm SiGe:C

IHP SG13G2Cu FEOL SG13G2 + Cu BEOL

IHP SG13SCu FEOL SG13S + Cu BEOL

IHP BEOL SG13

IHP SG13S + MEMRES Module

IHP SG13G3Cu 0.13µm SiGe:C

IHP SG13G3 FEOL SG13G3Cu + Al BEOL

ST

ST 28nm CMOSP28FDSOI

ST 28nm CMOS28FDSOI

ST 55nm BiCMOS055X

ST 65nm CMOS065

ST 130nm BiCMOS9MW

ST 130nm HCMOS9A

ST 130nm SOI H9SOI-FEM

ST 0.16µm BCD8sP

ST 0.16µm BCD8s-SOI

tsmc

TSMC 0.13µm BCD+ (12")

TSMC 0.13µm CMOS Log/MS/RF (G, LP)

TSMC 90nm CMOS Log/MS/RF (G ,LP)

TSMC 65nm CMOS Log/MS/RF (G, LP)

TSMC 40nm CMOS Log/MS/RF (G, LP)

TSMC 28nm CMOS Log/RF HPC/HPC+

TSMC 22nm CMOS Log/RF ULL

TSMC 16nm CMOS Log/RF FinFET Compact

TSMC 7nm CMOS Log/ RF FinFET

UMC

UMC L180 Logic GII, MM/RF

UMC L110AE Log/MM/RF

UMC L65N Log/MM/RF (LL)

UMC 40N Log/MM – LP

UMC 28N Log/MM – HPC

xfab

X-FAB XH035 0.35µm HV

X-FAB XH035 Noble Metal

X-FAB XH018 0.18µm HV NVM E-Flash

X-FAB XT018 0.18µm HV SOI

X-FAB XS018 0.18µm OPTO

X-FAB XP018 0.18 µm NVM

X-FAB XR013 0.13µm RF SOI/XIPD

X-FAB XT011 0.11µm HV SOI

X-FAB XMB10 MEMS

amf

AMF Si-Photonics

cea leti

CEA-leti Si-Photonics Si-310

CEA-Leti SiN-Photonics Si_3N_4-800

CEA-Leti MAD200 130nm NVM

CORNERSTONE

CORNERSTONE Si-Photonics 220 passives/actives

CORNERSTONE Si-Photonics 340 passives

CORNERSTONE Si-Photonics 500 passives

CORNERSTONE SiN-Photonics

CORNERSTONE Suspended-Si

CORNERSTONE Ge-on-Si

Fraunhofer
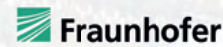
4H-SiC CMOS High Temperature Technology

imec

imec GaN-IC on SOI 200V/ 650V

imec Si-Photonics Passives+

imec Si-Photonics iSiPP50G

IMT

Glass microfluidics

LioniX INTERNATIONAL

LNX SiN-Photonics TriPleX VIS

LNX SiN-Photonics TriPleX 550

LNX SiN-Photonics TriPleX 850

Pragmatic

FlexIC Helvellyn 2.1.0

Science

MEMS PolyMUMPS

MEMS SOIMUMPS

MEMS PiezoMUMPS

teem PHOTONICS

Glass-Photonics IC ioNext-NIR

Glass-Photonics IC ioNext-VIS

Glass-Photonics IC WAFT

Tyndall National Institute

PiezoMEMS Single electrode layer stack

PiezoMEMS Dual electrode layer stack

United Monolithic Semiconductors

UMS GH25 0.25µm GaN HEMT

UMS GH15 0.15µm GaN HEMT

UMS PH10 GaAs pHEMT

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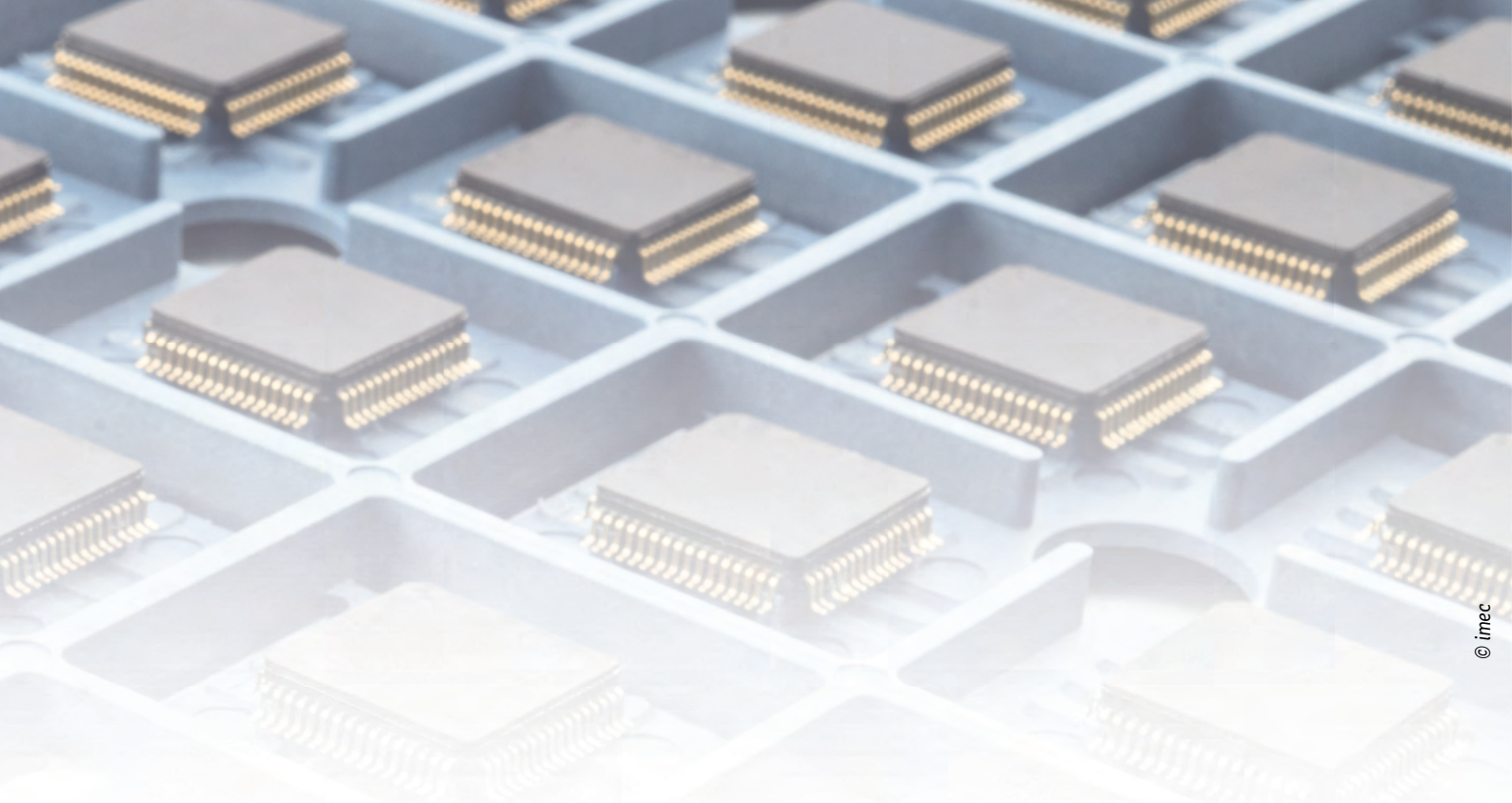
MULTI-LEVEL MASK SINGLE USER RUNS

Another technique to reduce the high mask costs is called Multi-Level Mask (MLM). With this technique the available mask area (for example 20mm × 20mm field for stepper equipment) is typically divided in four quadrants (4L/R : four layers per reticle) whereby each quadrant is filled with one design layer. As an example: one mask can contain four layers such as nwell, poly, ndiff and active. The total number of masks is therefore reduced by a factor of four. By adapting the lithographical procedure, it is possible to use one mask four times for the different layers by using the appropriate quadrants. This technique allows to significantly decrease the mask costs.

The advantages of using MLM single user runs are:
- lower mask costs
- an MLM run is organized for one customer
- it can be scheduled for any date since it does not depend on regular MPW runs
- a customer receives a few wafers, resulting in a few hundreds of prototypes

The MLM technique is preferred over MPW runs when the chip area becomes large and when the customer would like to get a higher number of prototypes. When the prototypes are successful, this mask set can be used under certain conditions for low-volume production.
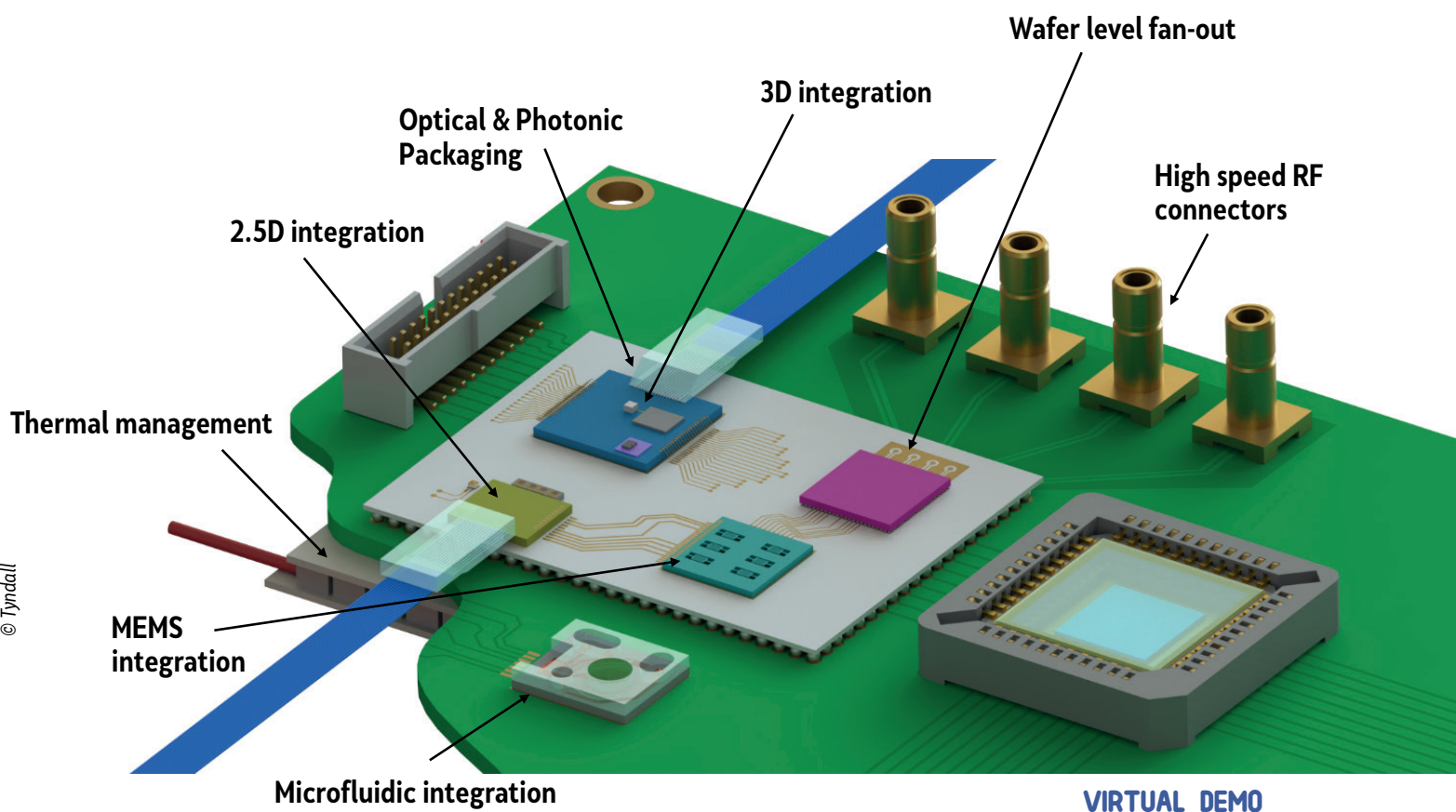
MLM runs are available for technologies from IHP, X-FAB and onsemi. As of 2022, onsemi does not offer MPW runs anymore and focuses on MLM.

PACKAGING

As a standard, EUROPRACTICE delivers unpackaged, untested prototype chips. However, EUROPRACTICE offers a low-cost, flexible and coordinated packaging service using industrial qualified packaging houses. A wide variety of **ceramic and plastic packages** are available, ranging from DILs (Dual-in-line) to PGAs (Pin Grid Array) and QFNs (Quad-Flat No-leads).

Side by side with world class partners and our long-term agreements, EUROPRACTICE boosts the deployment of your chip backend operations activities. This business environment is strengthened by a skilled team of in-house engineers who provide a reliable integrated service, from technical aspects up to logistics and supply chain management.

In addition, **photonics packaging** is offered by Tyndall. The photonics ecosystem continues to gather momentum attracting new users (from both academia and industry) and increasing the technical scope of the photonics offering via EUROPRACTICE. Finally, advanced packaging and system integration now complements EUROPRACTICE portfolio.

© Tyndall

2.5D integration

Optical & Photonic Packaging

3D integration

Wafer level fan-out

High speed RF connectors

Thermal management

MEMS integration

Microfluidic integration

ADVANCED PACKAGING AND SMART SYSTEM INTEGRATION

There is a growing demand for advanced packaging and system integration in the semiconductor industry. This trend has been fuelled by the need of a wide range of applications for better integration of more functionalities in a system-on-chip (SoC) and system-in-package (SiP). System integration is a scientific and engineering challenge of combining a variety of technology modules, such as microsystems, microelectronics, optics, photonics, MEMS, microfluidics and combinations thereof. Examples of system integration in the semiconductor industry are vast, such as high-speed high-density datacom, artificial intelligence (AI), Internet of Things (IoT), bio-medical devices, sensors and many more.

> Currently, the EUROPRACTICE portfolio is being extended with advanced packaging and system integration services enabling customers to realise complex multi-technology devices that can be upscaled from early-stage prototypes to volume manufacturing. This is achieved by adding specific processes or technologies in combination with the development of design rules and thereby facilitating advanced package design for system-on-chip integration.

EUROPRACTICE is showcasing the new system integration offer by means of virtual demonstrators, which are depicted on this page. They demonstrate how different building blocks or process modules make integration between multiple technologies possible. This covers advanced packaging of ASICs, photonics, MEMS, microfluidics and combinations of these technologies, from their design to their fabrication and integration.

System integration is made possible through EUROPRACTICE's unique access to a variety of specialized process modules, including 2.5/3D integration of ASICs and PICs through die stacking techniques using pick-and-place, flip-chip, BGAs, Cu pillars as well as silicon interposers. Access to wafer-level fan-out packaging is also provided, where dies from different sources or different technologies with varying thickness and size can be handled and packaged with one integration technology. Finally, add-on processes for noble metal finishes and microfluidic building blocks will be added to the technology portfolio, which are prerequisites for many bio-medical sensor devices. Most importantly, all solutions use industry-standard processes making them scalable to high volume and more cost effective.

FROM PROTOTYPES TO VOLUME PRODUCTION

Once successful ASIC prototyping has been completed based on the MPW principle, we can also provide a clear route to volume production (from low to mid-high volumes). During this upscaling process, you work closely together with one of the EUROPRACTICE partners, depending on the technology of your choice.

MIGRATION TO A FULL MASK SET

Based on a successful and validated prototype, the ASIC can be fabricated on a dedicated full mask set. One of the EUROPRACTICE partners takes care of the production of the first engineering wafers and organises the assembly in ceramic or plastic packages. Using their own bench tests, the designer can check the functionality of the ASIC produced on the full mask set.

DEVELOPMENT OF A TEST SOLUTION

When the device behaves according to the ASIC specifications, a test solution on an ATE (Automatic Test Equipment) platform is required to deliver electrical screened devices using a stable production test program. The test can be performed both on wafer level and on packaged devices. The goal is to screen the ASIC for manufacturing problems using the ATPG (Automatic Test Pattern Generation) and functional patterns. One of the EUROPRACTICE partners supports you during the development of single-site test solution as well as with a multi-site test solution when high-volume testing is required.

DEBUG AND CHARACTERIZATION

Before going into production, a characterisation test program checks if all the ASIC specifications meet the customer's expectations. Threshold values are defined for each tested parameter. The software tests all the IP blocks and functionalities in the ASIC, and the results are validated against the bench test results. A characterisation at Low (LT), Room (RT) and High (HT) temperature is performed on a number of (corner) samples together with statistical analysis (Cp and Cpk) to understand the sensitivity of the design against corner process variations.

QUALIFICATION

When the silicon is proven to be robust against process variations, the product qualification can start. Our partners can support you through the full qualification process using different kinds of qualification flows, including Automotive, Consumer, Industrial, Medical, Space, Military, Jedec and ESCC standards.
In this stage of the project, qualification boards must be developed for reliability tests and environmental tests.

YIELD IMPROVEMENT

EUROPRACTICE partners can perform yield analysis to determine critical points during the production and suggest the correct solution to maximise the yield. During the characterisation and qualification of the device on corner lots, the customer receives support in defining the final parameter windows. During the ramp-up phase, data of hundreds of wafers are analysed to check for yield incidents related to assembly and wafer production. The well-proven tool Examinator™ from Galaxy Semiconductor is used, enabling our engineers to perform fast data and yield analysis studies.

SUPPLY CHAIN MANAGEMENT

The responsible EUROPRACTICE partner will manage the full supply chain for you. This highly responsive service takes care of the planning processes with the different actors in the value chain during both engineering and production phases. Integrated logistics ensures the accurate achievement of the final delivery dates.

- **OSAT:** Amkor Technology, Aptasic, ASE, Chipbond, Greatek Electronics, Integra Technologies, JCET, KYEC, Microdul, MSEI, Swissbit, Synergie Cad, Winstek, YTEC
- **Assembly:** AEMtec, Alter Technology (Optocap), DISCO HI-TEC EUROPE, Kyocera, MAF, PacTech, QP Technologies, Reel Service, SERMA Microelectronics, Taipro Engineering, Teledyne e2v
- **Test:** Alter Technology Spain, EAG Laboratories, ISE Labs, Eurofins MASER, Microtest, Presto Engineering, RoodMicrotec, Salland Engineering
- **Photonics packaging:** Alter Technology, Bay Photonics, PHIX, PIXAPP, Tyndall
- **Library:** Aragio, ARM, Cadence, eMemory, Faraday, Synopsys
- **Rad test facility:** LLN, RADEF
- **Long-term storage:** TÜV NORD GROUP

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© Fraunhofer IIS

TRAINING IN DESIGN TOOLS AND TECHNOLOGIES

EUROPRACTICE provides training courses targeting academic staff and PhD students from European universities and research institutes. Unlike training courses which address single topics or individual design tools, the EUROPRACTICE training courses typically address a design flow which makes these training courses an efficient way to acquire new knowledge and ideally suited to new PhD students and junior engineers with a need to quickly become productive with a design flow.

Since the courses are based on the EUROPRACTICE design tools, PDKs and Technologies, participants will be able to directly apply the techniques learnt on the training course when they return back to their own organization and make full use of the EUROPRACTICE infrastructure in their innovation, research and training.

Courses include a strong element of practical sessions where participants have an opportunity to extensively practice the concepts described in lectures, and have access to experts who can answer questions about the concepts, design tools or technology processes discussed on the course.

Where a design flow is well supported by multiple vendors and/or processes, multiple course variants are offered that reflect the typical practice within European industry.

Over the last year, 30 courses provided training to 276 delegates, with 130 of these delegates being PhD students, many of whom will go on to become future industry and academic leaders.

Throughout 2023, courses transitioned from live instructor-led online training to physical in-person courses at one of the EUROPRACTICE partner sites. The return of in-person physical training has been welcomed by delegates because of the greater networking and learning opportunities that in-person physical training naturally allows.

WEBINARS

To introduce the constantly growing service portfolio and share valuable technology insights, EUROPRACTICE regularly develops and hosts highly successful webinars. These online events usually include informative presentations given by experts from world-leading companies, foundries or academic institutions, followed by a short Question & Answer session. All webinars are free of charge and open to a broad audience with different backgrounds.

In the past year, we hosted two webinar series now available on our YouTube channel:

Compound Semiconductors

This six-webinar series introduces the EUROPRACTICE community to the world of compound semiconductors and showcases the technologies already accessible through the EUROPRACTICE platform, such as SiC of Fraunhofer IISB, SiGe of IHP, GaAs of UMS, and GaN of imec and UMS. It also gives an overview of InP PIC technologies of JePPIX.

Pragmatic's Flexible Integrated Circuits

This series consists of two webinars and introduces participants to flexible integrated circuits (FlexIC) of Pragmatic, whose Multi-Project-Wafer (MPW) services and dedicated full-wafer runs are now available through EUROPRACTICE to users from academic institutions and research institutes.

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48 videos with our recorded webinars are available on the official YouTube channel of EUROPRACTICE Services, covering different technologies: Microfluidics, MEMS, Flexible Electronics, Graphene, Silicon-Photonics, advanced Photonics packaging and more.

In addition to the two series in 2023, we organised four individual webinars. One of them provided a general introduction to digital IC design and implementation. The other three focused on various aspects of IC design using Synopsys tools, covering Photonic Integrated Circuit (PIC) design, physics-based lithography process simulation, and analog design.
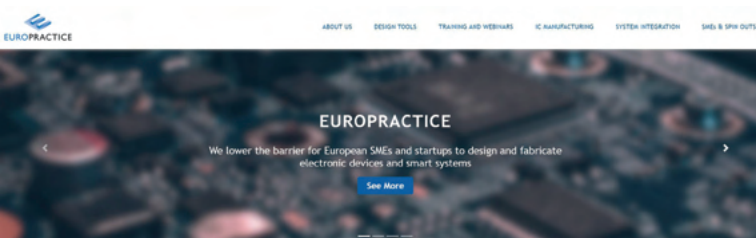
EUROPRACTICE webinars remain highly popular. Last year, the live-stream sessions were attended by approximately 150 delegates each.

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COMMUNICATION AND OUTREACH

At EUROPRACTICE, we use a wide range of communication channels to increase awareness about our services and deliver the latest updates to both existing and potential users. Among online platforms, our web portal and social media channels play a primary role.

WEB PORTAL

The **General Portal europractice.com** is the main entry point for EUROPRACTICE services, where you can find all the information you require. For further details on one of the aspects of our portfolio, the portal will redirect you to:

⤷ **Design Tool & Training website europractice.stfc.ac.uk** with the latest information related to EUROPRACTICE membership, purchase of design tool licenses, upcoming training courses and webinars;

⤷ **Technology & Fabrication website europractice-ic.com** with detailed information on the MPW offer, run schedules, and pricing.

SOCIAL MEDIA

We are happy to see that our EUROPRACTICE community on LinkedIn and YouTube is growing. Following our accounts is a great way to stay informed about the latest service portfolio additions and share your experience with EUROPRACTICE.

On **LinkedIn**, we do not just publish announcements of new technologies and services, but we also give visibility to our customers by publishing their testimonials and technical user stories. At the beginning of 2024, our LinkedIn community counted nearly 3.500 followers.

The **YouTube** channel EUROPRACTICE Services gives a great opportunity to watch our webinar recordings. In February 2024, the channel had approximately 70.000 views and almost 1.400 subscribers.

CONFERENCES AND EXHIBITIONS

Every year, the EUROPRACTICE team participates in various scientific conferences, industrial trade shows and fairs to present our services to existing customers and to attract new prospects.

In 2023, we attended 18 events. For priority events, our consortium members delivered talks and staffed dedicated booths using promotional material designed in the well-recognisable bright-colour palette of EUROPRACTICE.

A notable addition to our activities became organizing EUROPRACTICE workshops at prominent European conferences. At ESSCIRC-ESSDERC in September 2023, we hosted a workshop focusing on Design IP Sharing and Chiplets. This year, at DATE 2024, we are preparing a workshop entitled "Tips and Tricks for a Successful Multi-Project-Wafer (MPW) Chip."

LinkedIn announcement of our workshop at ESSCIRC-ESSDERC 2023

EUROPRACTICE team at the Chips JU launch event

EUROPRACTICE book display at ISSCC 2023

In 2024, we will attend at least the following conferences and fairs:

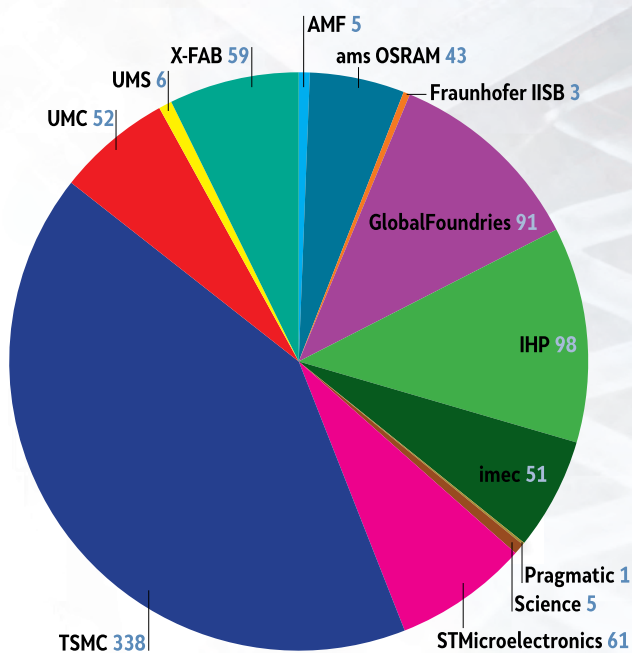| DATE 2024	Valencia, Spain	25-27 March
PRIME 2024	Larnaca, Cyprus	9-12 June
SMACD 2024	Volos, Greece	2-5 July
ESSERC 2024	Bruges, Belgium	9-12 September
ISSCC 2025	San Francisco, US	16-20 February (TBD)

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RESULTS 2023:
MPW PROTOTYPING

INCREASE IN NUMBER OF SUBMITTED DESIGNS

We are delighted to see that the number of designs on EUROPRACTICE MPW runs has grown over the previous year. In 2023, our customers submitted a total of 813 designs for fabrication, indicating a substantial 10% growth compared to the results of 2022. This increase indicates that the rich EUROPRACTICE MPW offer effectively addresses diverse requirements of our customers, ensuring the continuous and successful support of European academia and industry.

As in previous years, the majority of designs (78%) were submitted by European customers. Within Europe, universities and research institutes contributed 65% of the total submissions in the region, while the industry, primarily SMEs and startups, accounted for 13%.
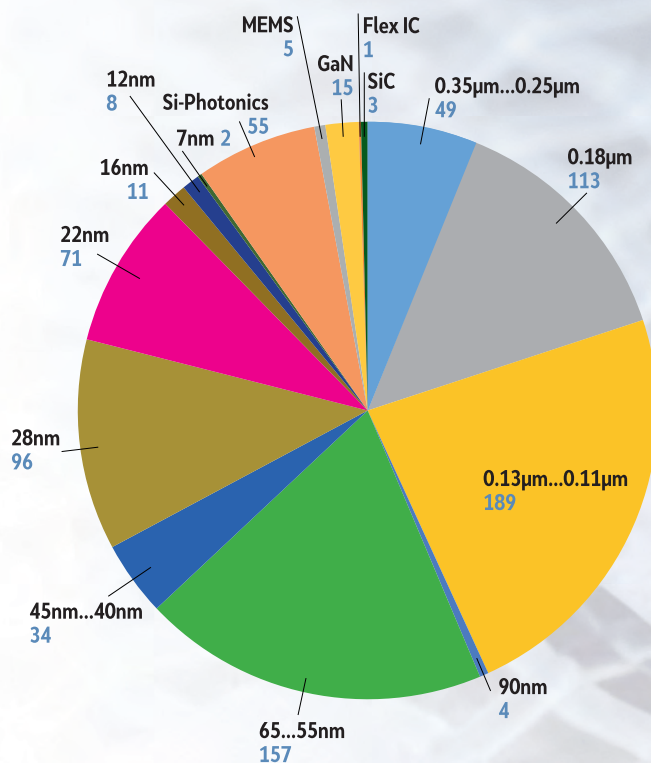
Research outside Europe 15%

European industry 13%

European research institutes 25%

Industry outside Europe 7%

European universities 40%

MPW designs in 2023

ACCESS TO A DIVERSE RANGE OF FOUNDRIES

Similar to previous years, the majority of designs submitted in 2023 were manufactured by TSMC, a leading foundry in the global industry. Notably, the second place is occupied by a European R&D fab IHP, whose numbers have more than doubled, surpassing GlobalFoundries. Imec is another European research centre that has also demonstrated a good increase in the number of prototyped designs. Overall, European foundries, including STMicroelectronics and X-FAB, have shown impressive growth in the number of prototyped designs.

We are pleased to highlight that EUROPRACTICE users have successfully started prototyping in the technologies of the foundries that have recently joined EUROPRACTICE, such as Pragmatic, UMS, and Fraunhofer IISB.
.

AMF 5
ams OSRAM 43
X-FAB 59
UMS 6
Fraunhofer IISB 3
UMC 52
GlobalFoundries 91
IHP 98
imec 51
Pragmatic 1
Science 5
TSMC 338
STMicroelectronics 61

Number of fabricated designs in 2023 per foundry

Number of fabricated designs in 2023 per technology (node)
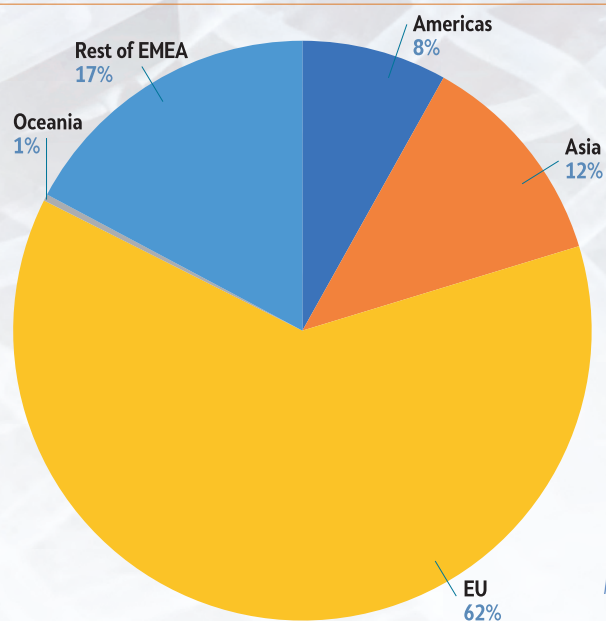
UNPARALLELED TECHNOLOGY MIX

EUROPRACTICE provides access to a very diverse range of technologies, encompassing advanced nodes, older technology nodes, and More-than-Moore technologies, each contributing significantly to the overall volume. The older technology nodes, ranging from 0.11µm to 0.35µm, continue to maintain popularity, constituting around 43% of the submitted designs. Among the more advanced nodes, the 65nm technology and its associated nodes are the most popular, with 157 prototypes fabricated.

There is a notable upward trend in the adoption of advanced technologies among EUROPRACTICE users. Specifically, there has been an increase in the number of users prototyping in 12-nm FinFET technologies offered by TSMC and GlobalFoundries, as well as 28-nm technologies provided by TSMC (HPC+) and STMicroelectronics (FD-SOI).
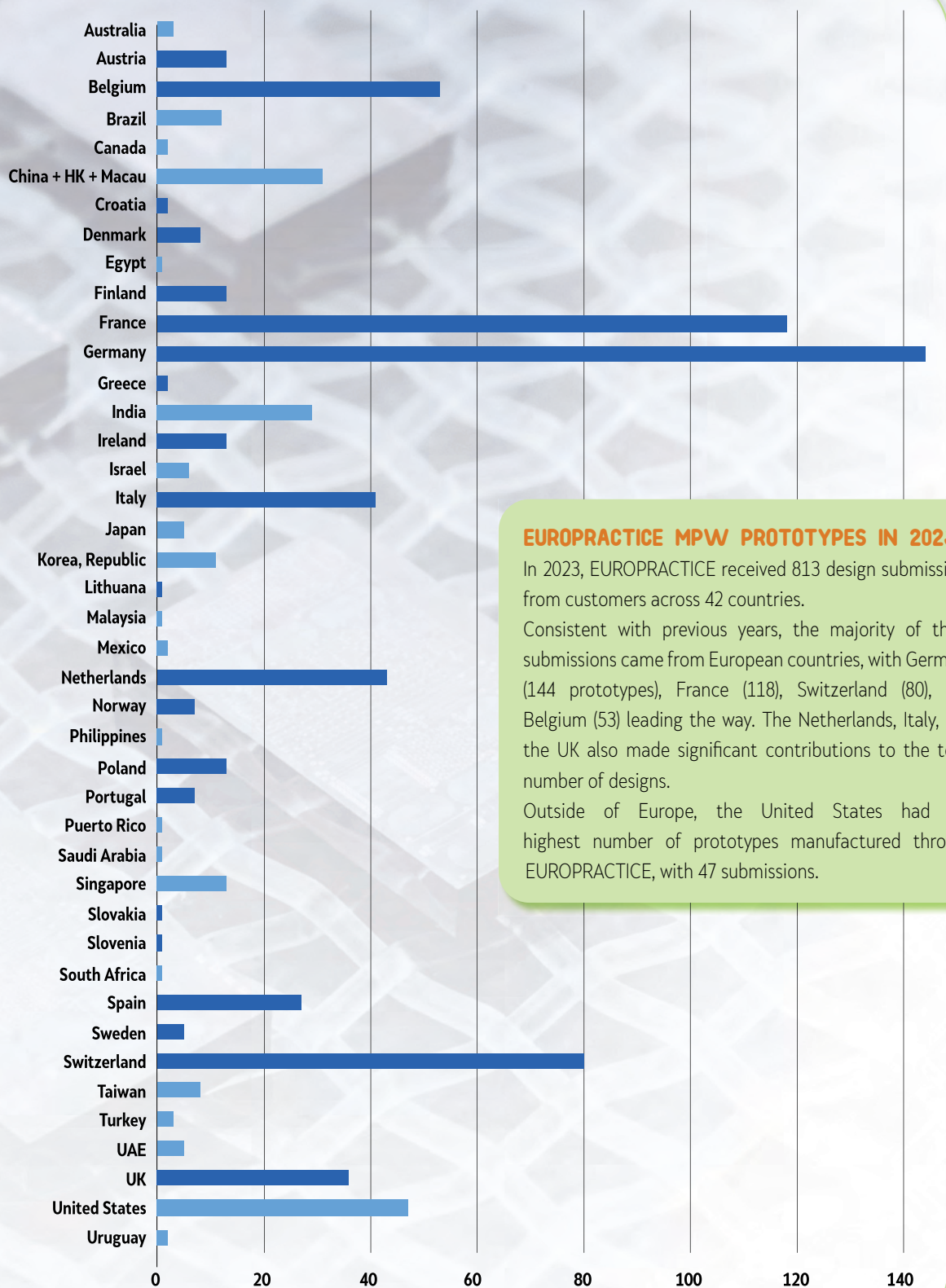
The popularity of More-than-Moore technologies has also slightly increased. This should be attributed in part to the first prototypes manufactured in technologies recently incorporated into the EUROPRACTICE portfolio. This includes Flexible Electronics (FlexIC) by Pragmatic, GaN offered by UMS, and SiC by Fraunhofer IISB.

GEOGRAPHICAL DISTRIBUTION

In line with previous years, over three-quarters of the designs fabricated in 2023 originated from Europe and the EMEA (Europe, Middle East and Africa) region, with the proportion of EU designs increasing to 62%. A moderate number of customers from Asia also used EUROPRACTICE prototyping services in 2023. The remaining 9% of prototypes were manufactured for customers from the Americas (mainly the US) and Australia.

Geographical distribution of MPW designs in 2023

Chart: Countries with bar values (number of MPW prototypes in 2023)
- Australia
- Austria
- Belgium
- Brazil
- Canada
- China + HK + Macau
- Croatia
- Denmark
- Egypt
- Finland
- France
- Germany
- Greece
- India
- Ireland
- Israel
- Italy
- Japan
- Korea, Republic
- Lithuana
- Malaysia
- Mexico
- Netherlands
- Norway
- Philippines
- Poland
- Portugal
- Puerto Rico
- Saudi Arabia
- Singapore
- Slovakia
- Slovenia
- South Africa
- Spain
- Sweden
- Switzerland
- Taiwan
- Turkey
- UAE
- UK
- United States
- Uruguay

X-axis: 0, 20, 40, 60, 80, 100, 120, 140

EUROPRACTICE MPW PROTOTYPES IN 2023

In 2023, EUROPRACTICE received 813 design submissions from customers across 42 countries.

Consistent with previous years, the majority of these submissions came from European countries, with Germany (144 prototypes), France (118), Switzerland (80), and Belgium (53) leading the way. The Netherlands, Italy, and the UK also made significant contributions to the total number of designs.

Outside of Europe, the United States had the highest number of prototypes manufactured through EUROPRACTICE, with 47 submissions.

USER STORIES
ON PROTOTYPED
DESIGNS

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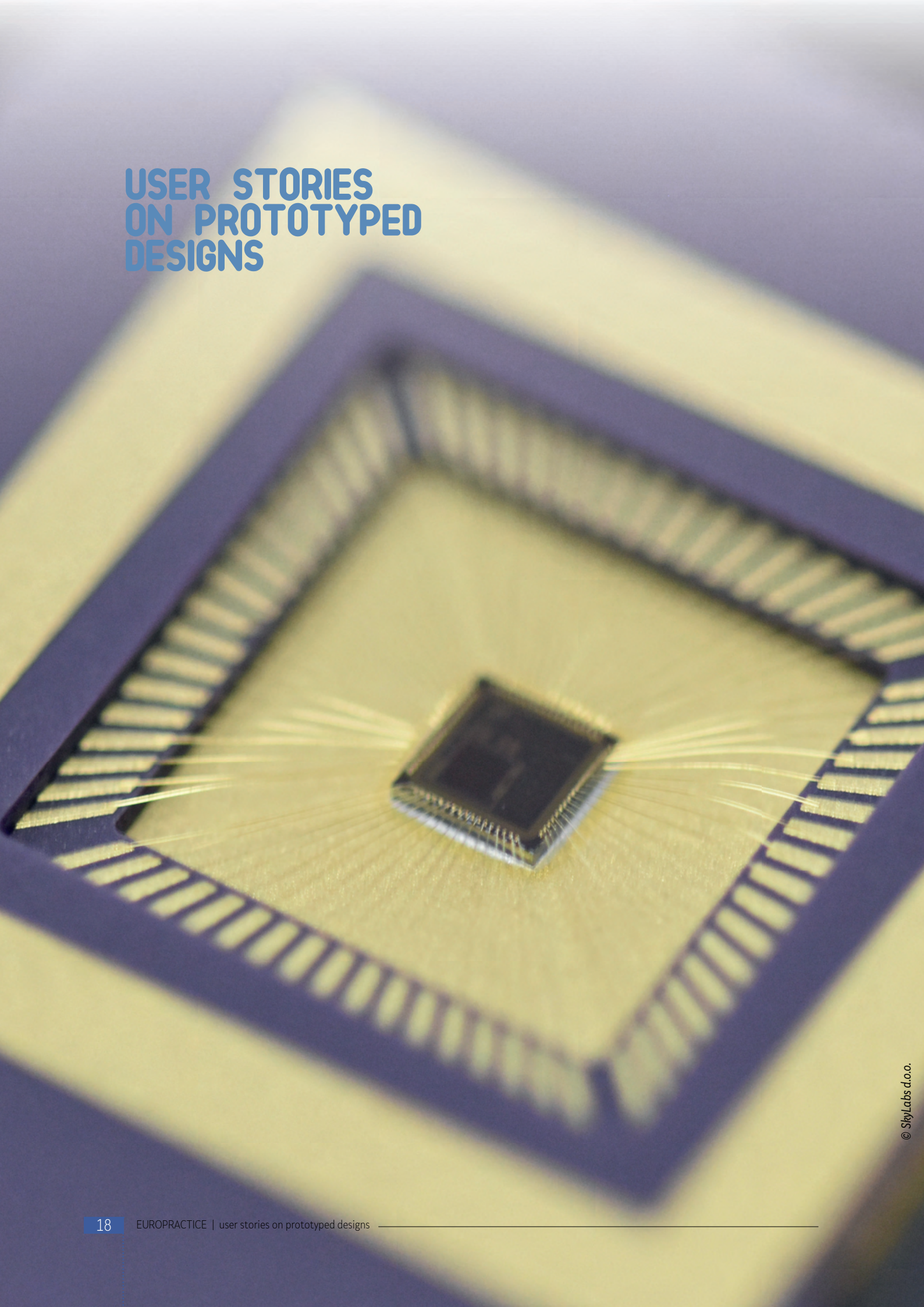
FASP_04 ASIC for the Transition Radiation Detector with two-dimensional position information for CBM experiment at FAIR

National Institute for Research and Development in Physics and Nuclear Engineering – Horia Hulubei, Măgurele, Romania

Contacts:	Dr.Vasile Catanescu
	Claudiu Schiaua
E-mail:	catanesc@nipne.ro, schiaua@nipne.ro
Technology:	ams 0.35µm CMOS C35B4C3 4M
Die Size:	3.4mm x 4mm
Design Tools:	Cadence
Application Area:	Detectors used in basic research experiments

Introduction

The Fast Analog Signal Processor (FASP) ASIC was designed for Compressed Baryonic Matter (CBM) at the future acceleration facility FAIR, Darmstadt, Germany. The ASICs will be integrated into the Front-End Electronics (FEE) of the Transition Radiation Detector with two-dimensional position information (TRD-2D).

Description

The FASP_ASIC has 16 self-triggered analogic red-out channels, with mixed-signal type circuits for processing the signals provided by 16 consecutive readout pads of the TRD-2D. The ASIC requires interconnection for a continuous readout of the whole active area of the chamber. The signals produced by a charged particle hit in the chamber are distributed on few consecutive pads and processed together, in a self-triggered mode (the channel with the highest signal enables also the processing of the signal of the neighbours). A mixed-signal circuitry is generated to both inter-channel communication within one ASIC as well as between neighbouring ASICs.

For each processed input signal, two output signals are delivered:
a) a flat top analog (peak-sense) signal with adjustable time interval. Two versions, including an option for flat-top or semi-Gaussian output, were also designed and produced.
b) a logical signal lasting 14 clock periods.

Both types of FASP_ASIC outputs are suitable for driving a wide range of ASIC or commercial analog-to-digital converters.
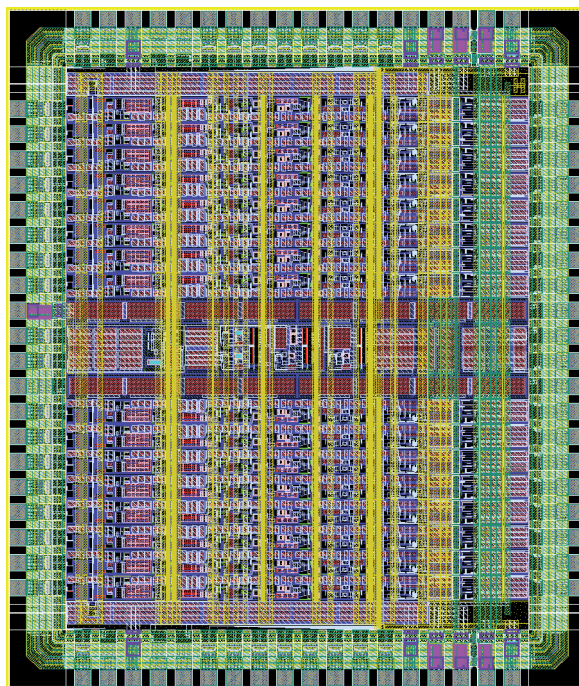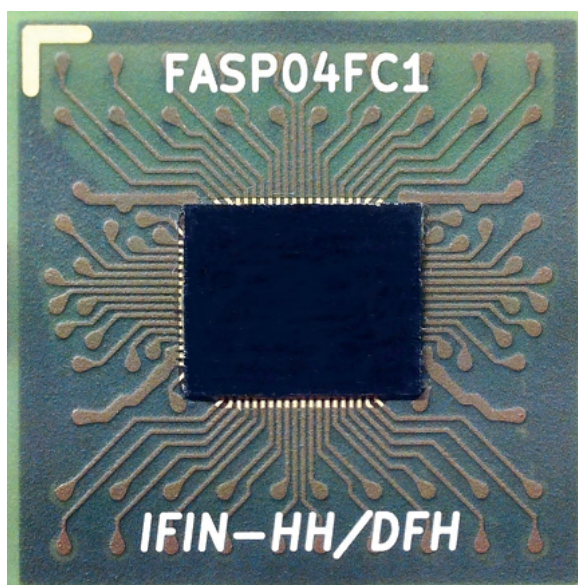

Fig.1: Layout of FASP_04 ASIC.

Fig.2: FASP_04 PCB substrate for flip-chip connection.

Each FASP_ASIC channel contains:
- Charge sensitive preamplifier
- Pole-zero circuit
- Two stages of 2nd order RC filters
- Peak-detector circuit: It detects and maintains the peak value of the RC filters output signal, providing the possibility of two selectable types of the output signal, a semi-Gaussian or/and the peak value (flat-top)
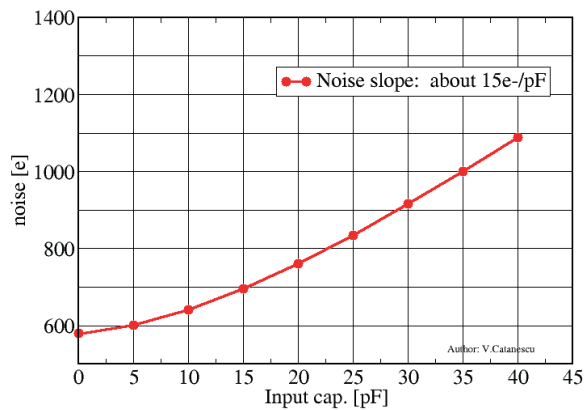
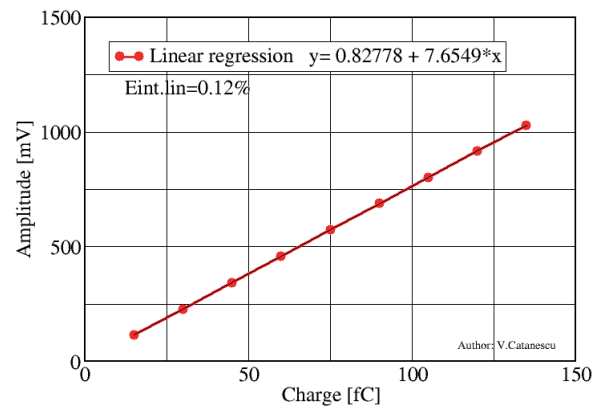Fig.3: Channel noise variations with input capacitance.

Fig.4: Channel integral nonlinearity.

• Logic circuitry: This part implements self-trigger signals, generating the logic signals for ASIC inter-channel communications and interconnection between the neighbouring ASICs. It also provides the logic signals necessary to connect and synchronize with external ASIC or commercial ADCs

Results

Detailed simulations (i.e. typical, corner, Monte Carlo) were carried out, in schematic and layout. The results of the manufactured chips are presented in the table below.

Detector pad capacitance	25pF
Positive input charge range	0.15fC - 165fC
Input pulse rate	max 2 MHz
Channel gain	6.2 mV/fC
RC filter shaping time	100 ns
Channel noise ($C_{det.pad.}$=25pF)	940 e
Noise variation with det. pad cap.	15e/pF
Channel integral nonlinearity	
semi-Gaussian output	0.12%
peak-sense output	0.06%
Analog output range	0 - 1 V
DC adj. output level	0.2 V - 0.5 V
Peak-sense output plateau width	16 Tck
Semi-Gaussian output FWHM	290 ns
External clock frequency	max 80 MHZ

Why EUROPRACTICE?

The EUROPRACTICE service offers Academic Institutions and Universities extremely useful opportunities for research and the training of specialists in microelectronics at affordable prices.
The MPW submission system and the mini@sic programs allow the production of prototypes at low costs in a reasonable time to test the specific solutions adopted by the user.
EURPORACTICE is the right interface between researchers and students developing microcircuits, between software suppliers and foundries. Access to new technological developments is made simple and fast, offering support and qualified information to users of EUROPRACTICE services.

Acknowledgements

CMOS-MEMS Resonators for ultra-sensitive VOCs detection

University of the Balearic Islands, Palma, Illes Balears, Spain

Contact:	Rafel Perelló-Roig
E-mail:	rafel.perello@uib.es
Technology:	ams OSRAM 0.35µm CMOS C35B4C3
Die Size:	0.7mm x 0.4 mm
Design Tools:	Cadence Virtuoso
Application Area:	Medical / Health

Introduction

Non-invasive health diagnosis through monitoring the volatile organic compounds (VOCs) present in the exhaled human breath has gained much attention in the biomedical field. Still, with more than 800 different compounds, these appear in concentrations below parts-per-million (ppm) for which sub-ppm and highly selective sensing elements are required.

CMOS-MEMS resonators, micromechanical structures fabricated using CMOS technology processes, have been proven as ultra-sensitive mass sensing elements that also bring added value with monolithic integration in single-chip applications. The sensing principle relies on measuring the downshift of resonance frequency after having deposited a mass on the mechanical structure. We propose to extend such solution to VOCs detection by using an active organic molecule-based sensing layer, whose fabrication is batch compatible in line with the overall System-on-Chip application goal, to capture the analytes of interest.

Description

This work presents a MEMS plate resonator oriented to VOCs sensing and fabricated using the ams OSRAM C35 CMOS technology that co-integrates a sustaining amplifier for self-sustained oscillation operation (see Figure 1) for which a frequency-related quasi-digital output signal is provided. The designed device uses an electrostatic actuation scheme and capacitive readout to transduce the mechanical vibration into a capacitive current.

The MEMS resonators (Figure 2) are fabricated using the BEOL top metal layer, i.e. 850-nm thick, and feature a platform size of 10µm wide and 41µm long, with four anchoring points realized by folded flexure beams 800-nm wide. A wet-etching post-processing step, performed at our laboratory facilities,
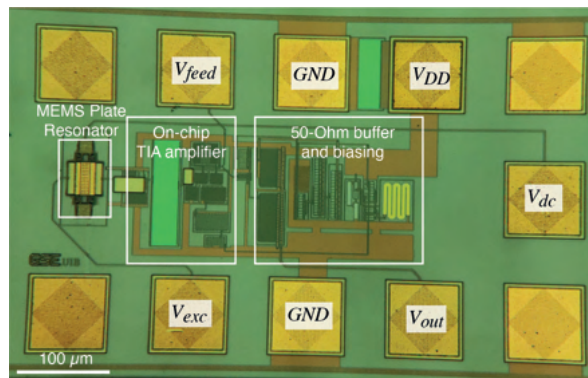

Fig.1: Optical image of the CMOS-MEMS chip after ENIG gold plating, the resonator is on-chip integrated with the CMOS sustaining amplifier.
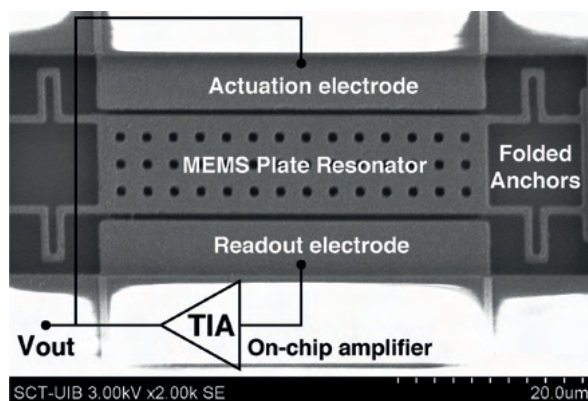

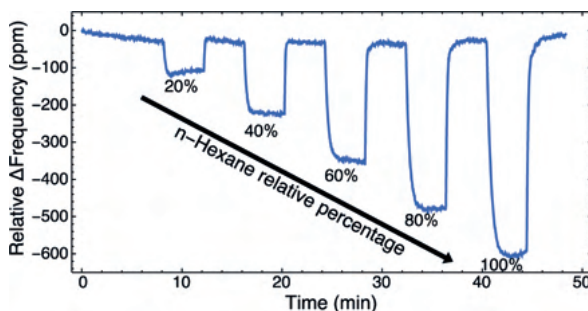Fig.2: SEM image of the integrated CMOS-MEMS plate resonator.

Fig.3: Measured sensor response to n-heane exposure from 0% to 100% of partial vapor pressure at 22℃.

is required to remove the sacrificial silicon oxide and release the moving parts, fully compatible with batch production. Also, an electroless nickel gold immersion coating (ENIG) is used to deposit a 100-nm gold layer to enhance the surface chemical capabilities and allow for thiol-based organic molecule functionalization.

Results

The fabricated CMOS-MEMS oscillator demonstrated self-sustained operation with a frequency of 2.21 MHz for a biasing voltage of 20 V and delivered a frequency stability, measured through the Allan deviation, of 0.35ppm for 100ms integration. The sensor was experimentally characterized with n-hexane injections at different concentration (see Figure 3) using a custom-made gas calibration setup. Experimental evidence shows a measured frequency downshift proportional to the n-hexane concentration with a sensitivity of 5.9ppm/%. Future work envisages modifying the functional group of the organic molecule to achieve selective caption to various analytes of interest.

Why EUROPRACTICE?

Using the ams OSRAM C35 CMOS fabrication process through EUROPRACTICE was key for the development of this project since it allows fast feedback between the design and the experimental results to validate such design at a reasonable price. Also, when using the metal layers to define MEMS structure in a non-conventional way, it is essential to access the foundry easily.

Acknowledgements

References

[1] R. Perelló-Roig, J. Verd, S. Bota, B. Soberats, A. Costa and J. Segura, "1-octadecanethiol Sam on CMOS-MEMS Gold-Plated Resonator via Dip-Cast for VOCS Sensing," 2023 IEEE 36th International Conference on Micro Electro Mechanical Systems (MEMS), Munich, Germany, 2023, pp. 795-798.

[2] R. Perelló-Roig, J. Verd, S. Bota and J. Segura, "Detailed analysis of flow-induced thermal mechanisms in sub-micron MEMS-based VOC biosensors: A design solution for the nanometer scale," 2022 IEEE 22nd International Conference on Nanotechnology (NANO), Palma de Mallorca, Spain, 2022, pp. 149-152.

ADELIA (Analog Deep Learning Inference Accelerator) Gen 2
Fraunhofer IIS, Erlangen, Germany

Contact: Dr. María Loreto Mateu Sáez
E-mail: loreto.mateu@iis.fraunhofer.de
Technology: GlobalFoundries 22nm FD-SOI 22FDX
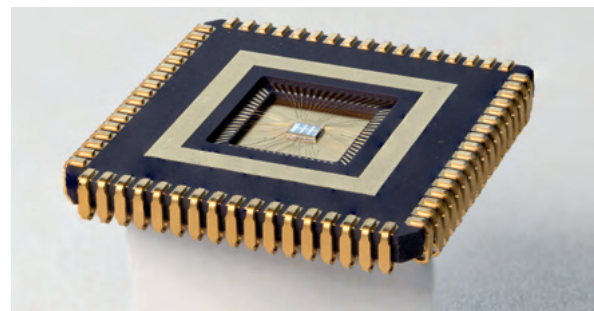**Die Size:** 2mm x 1.5 mm
Application Area: AI

Fig.1: ADELIA Gen 2 ASIC in 22FDX® with 6 analog in-memory computing cores.

Introduction

Since the requirements for cloud and near-sensor or in-sensor computing in terms of performance are different, new architectures, circuits and software tools are explored. While cloud platforms employ GPUs and TPUs, smart sensor solutions can leverage inference accelerators to extend their battery run time. Especially inference accelerators with analog in-memory computing (IMC), as the one presented here, that target ultra-low energy and low latency applications, are very well suited to compute sensor data with deep neural networks (DNNs). Applications in the market segments of media, healthcare, automotive, smart wearables, industrial electronics or consumer electronics for intelligent prosthetics, fitness tracking, predictive maintenance, audio classification, etc., are potential use cases for such IMC accelerators.

The variance of the analog storage of the weights and the MAC computation does not impact the accuracy of the designed ASIC, thanks to our hardware-aware training tool. Moreover, the developed mapper and compiler are used to transfer the DNN trained models to the ASIC.

Description

The ADELIA (Analog Deep Learning Inference Accelerator) Gen 2 is a multi-core inference accelerator with SRAM based analog in-memory computing cores designed in 22FDX® for low energy and low latency edge AI applications. It can perform inferences of

Fig.2: Voice activity detection demonstrator of the ADELIA Gen 2 ASIC.

deep neural networks. Each of the six cores has a crossbar array with 256 rows and 64 columns, an input memory (8 kB) for storing the data to be processed by the core, a weight memory (8 kB) for storing the weights of the layers to be computed by the core and an instruction memory (1 kB) for storing the configuration parameters needed for the execution of an inference. A bridge fabric takes care of the data transfer between the cores.

Each of the cores can compute 1D and 2D convolutions, with a maximum kernel length of 256, and fully connected layers. The supported weight quantization is 3, 5 and 9 bits including sign. The current activation function employed is ReLU.

Results

The ASIC has been characterized over 0 – 80°C temperature range and its functionality has been verified. The ASIC has been tested with a VAD CNN model with 5 convolutional layers and 2 fully connected layers with 19,760 weights, 775,497 MAC operations and 6,505 neurons overall.

The targeted accuracy for the VAD use case was 80%. The CNN model for VAD use case trained with our in-house hardware aware training (HAT) tool achieved 89% accuracy with floating point precision for the weights and 83.3% accuracy with 3-bit quantization for the weights, taking into account the variations of the hardware. The ASIC, over the temperature range of interest, achieves over 80% accuracy. The inference time is 1ms and the power consumption is under 0.5mW.

The ASIC has been successfully integrated into a demonstrator including a Raspberry Pi that performs the Mel Spectrogram of the input audio signal. The demonstrator can classify either live audio data from a microphone or recorded audio data stored on an SD card.

Why EUROPRACTICE?

EUROPRACTICE Services allows us to get access to GlobalFoundries technologies. The division Smart Sensing and Electronics at Fraunhofer IIS has, therefore, been able to acquire over 7 years experience in IC design with the 22FDX® technology. Thanks to the EUROPACTICE Services, we have been able to tapeout our IC designs, like in this case for the ANDANTE project, in a mini@sic run and also get packaged samples.

Acknowledgements

References

[1] Mateu, Loreto, et al. "Tools and Methodologies for Edge-AI Mixed-Signal Inference Accelerators." Embedded Artificial Intelligence: Devices, Embedded Systems, and Industrial Applications (2023): 25.

[2] Müller, Roland, Loreto Mateu, and Ralf Brederlow. "Analog/Mixed-Signal Standard Cell Based Approach for Automated Circuit Generation of Neural Network Accelerators." 2023 38th Conference on Design of Circuits and Integrated Systems (DCIS). IEEE, 2023.

[3] ANDANTE web page: www.andante-ai.eu

Components for Analog Neural Network Inference Accelerators

Institute of Electrical and Optical Communications, University of Stuttgart, Stuttgart, Germany

Contacts:	Jakob Finkbeiner, Raphael Nägele
E-mail:	jakob.finkbeiner@int.uni-stuttgart.de
Technology:	GlobalFoundries 22nm FD-SOI 22FDX
Die Size:	1mm x 1mm
Design Tools:	Cadence Virtuoso
Application Area:	AI

Fig.1: Photograph of the fabricated ASIC. It is placed into the cavity of a high-frequency printed circuit board and connected with wire bonds.

Introduction

Many applications today benefit from artificial neural networks (ANNs). The large computational effort they require consumes a lot of energy, making them difficult to handle in edge devices like smartphones and sensors. Specialized ANN accelerators try to solve this problem by using optimized architectures and circuits. We have developed highly efficient analog circuits for such ANN accelerators.

Description

The multiply-accumulate (MAC) operation and the ReLU activation function are the two essential operations of ANNs. Our MAC unit design employs only four transistors and one memory capacitor and consumes less than 1 fJ per MAC operation. The innovative analog implementation of the activation function allows us to flexibly adjust the threshold and slope of the ReLU activation function to the requirements of ANNs.

Results

We have designed an ASIC (Fig 1.) that contains our analog MAC and ReLU circuit. The measurement results demonstrate flexible, energy- and area-efficient circuits with high possible throughput for ANN inference. Future work will show a multi-layer analog ANN accelerator where the two operations are combined.
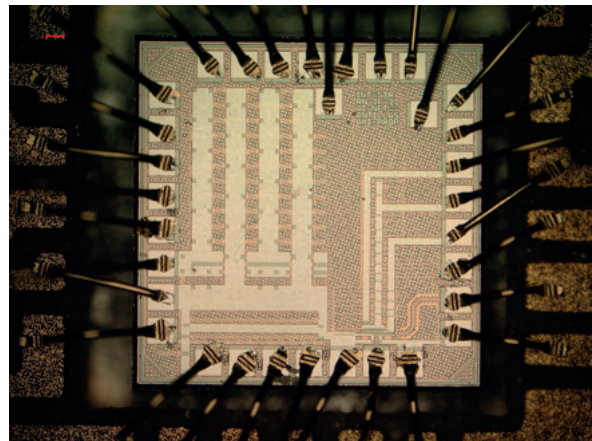
Why EUROPRACTICE?

EUROPRACTICE gives us access to state-of-the-art technologies and provides the tools to design our ASIC and printed circuit boards. They offer quick and helpful support during the tape-out process of the ASIC. Without all this help, we would not be able to achieve our ambitious goals. We are very grateful for this and look forward to working together in the future.

Acknowledgements

References

[1] R. Nägele, J. Finkbeiner, M. Grözing and M. Berroth, "Design of an Energy Efficient Analog Two-Quadrant Multiplier Cell Operating in Weak Inversion," 2022 20th IEEE Interregional NEWCAS Conference (NEWCAS)

[2] J. Finkbeiner, R. Nägele, M. Grözing and M. Berroth, "Design of an Energy Efficient Voltage-to-Time Converter with Rectified Linear Unit Characteristics for Artificial Neural Networks," 2022 20th IEEE Interregional NEWCAS Conference (NEWCAS)

[3] R. Nägele, J. Finkbeiner, V. Stadtlander, M. Grözing and M. Berroth, "Analog Multiply-Accumulate Cell with Multi-Bit Resolution for All-Analog AI Inference Accelerators," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 70, no. 9, pp. 3509-3521, 2023

High-Speed SAR ADCs for use in Sub-ADC-Based Systems

Institute of Microelectronics, University of Ulm, Ulm, Germany

Contacts:	Jonathan Ungethüm, Michael Pietzko, Dr. John G. Kauffman, Dr. Joachim Becker, Prof. Dr. Maurits Ortmanns
E-mail:	jonathan.ungethuem@uni-ulm.de
Technology:	GlobalFoundries 22nm FD-SOI 22FDX
Die Size:	1.25mm x 1.25mm
Design Tools:	Cadence Virtuoso, Spectre; Siemens Calibre
Application Area:	Datacom / Telecom

Introduction

Modern communication standards require medium to high-resolution, high-bandwidth digitizers. In this field, sub-ADC-based systems such as continuous-time (CT) pipelined ADCs (CTPs), time-interleaved (TI) ADCs or CT Delta-Sigma-modulators (DSMs) are often employed. These systems often require low-to-medium resolution, high-speed quantizers to achieve the required resolution and bandwidth. SAR ADCs have become good candidates for such systems, thanks to technology scaling. However, limited operation speed due to serial operation of the SAR loop still is a drawback when compared to Flash quantizers. This issue can be mitigated using parallelization techniques at the cost of increased number of error sources requiring extensive calibration. In our design, we implemented two ADCs: a 1.6GSps 6-bit asynchronous SAR and a 600MSps 10-bit asynchronous SAR with preloading Flash. The 10-bit ASAR is currently submitted for publication, while the former has been presented at ESSCIRC 2023. As such, the following description refers solely to the 1.6GSps 6-bit SAR ADC.

Description

Two 6-bit SAR ADC Channels were implemented to test the suitability of the ADC in a 2X-TI ADC. An improved comparator and logic design allow to detect slow decisions. This information can be used to increase possible conversion speed compared to conventional single-loop implementations. To minimize the offset error, which can become problematic especially in CTPs and CT-DSMs, chopping was implemented at the ADC input and output. A custom capacitive DAC array was designed to achieve good matching while keeping the switched input capacitance as low as 36.1fF including parasitics.
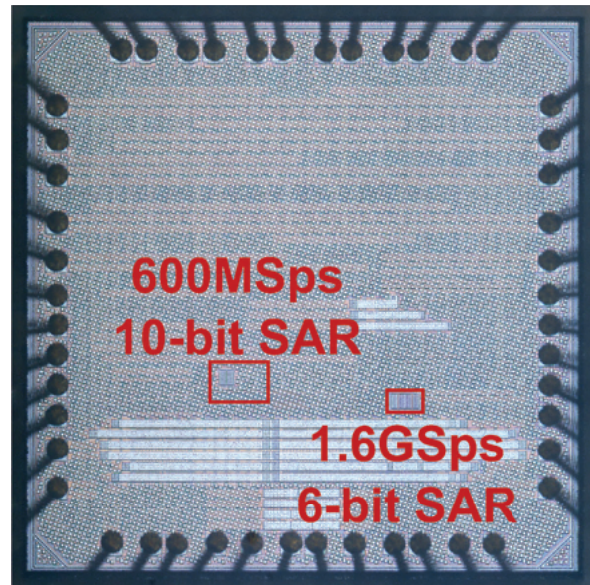

Fig.1: Die photograph.
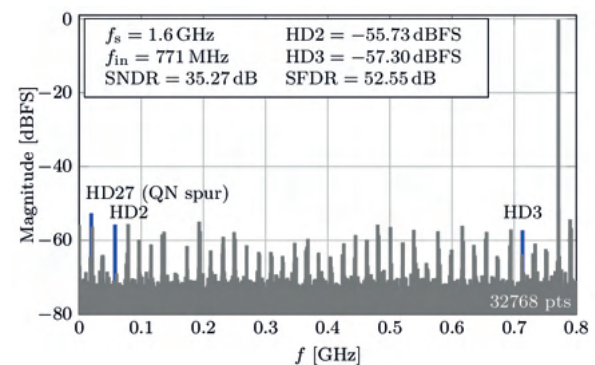

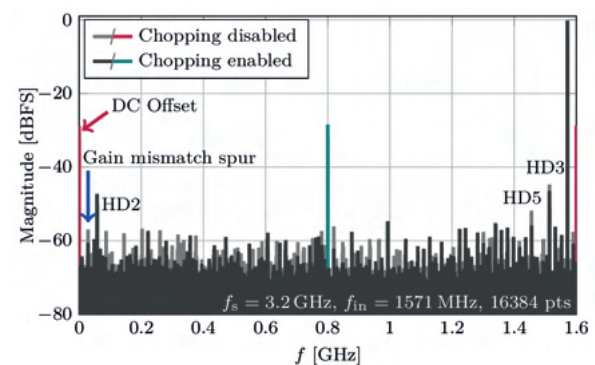Fig.2: Output spectrum of the single-channel SAR ADC operating at 1.6GSps, modified from [1].

Fig.3: Output spectrum of the 2X-TI SAR ADC with and without chopping enabled, modified from [1].

Results

The single-channel ADC occupies an area of 724µm² and achieves a resolution of 5.57 ENOB at 1.6 GSps while consuming 1.89 mW from a 850 mV supply. Evaluating the output of the

2X-TI ADC shows the effectiveness of chopping: Enabling chopping at 800 MHz (half of the sub-ADC's sampling frequency) moves the offset-induced spurs from DC and 1.6 GHz to 800 MHz without introducing further errors. The achieved results show the functionality of the proposed approaches. Due to the low area consumption and easy driveability, the ADC is suitable for use in sub-ADC-based systems.

Why EUROPRACTICE?

As an academic research team, our mission is to advance integrated mixed-signal circuits and systems, which need manufacturing and validation by hardware measurements to make an impact to the community. EUROPRACTICE offers the complete tool chain, access and support to a large number of technologies, which makes our research possible at all. The mini@sic runs and various packaging options offered by EUROPRACTICE are ideal for us, as limited chip size can be realized for a reasonably low cost.

Acknowledgements

References

[1] J. Ungethüm, M. Pietzko, A. Abdelaal, J. G. Kauffman and M. Ortmanns, "A Chopped 6-bit 1.6 GS/s SAR ADC Utilizing Slow Decision Information in 22 nm FDSOI," ESSCIRC 2023-IEEE 49th European Solid State Circuits Conference (ESSCIRC), Lisbon, Portugal, 2023, pp. 141-144, doi: 10.1109/ESSCIRC59616.2023.10268704.

Low noise transimpedance amplifier for infrared detectors
ChipCraft Sp z o.o., Warsaw, Poland

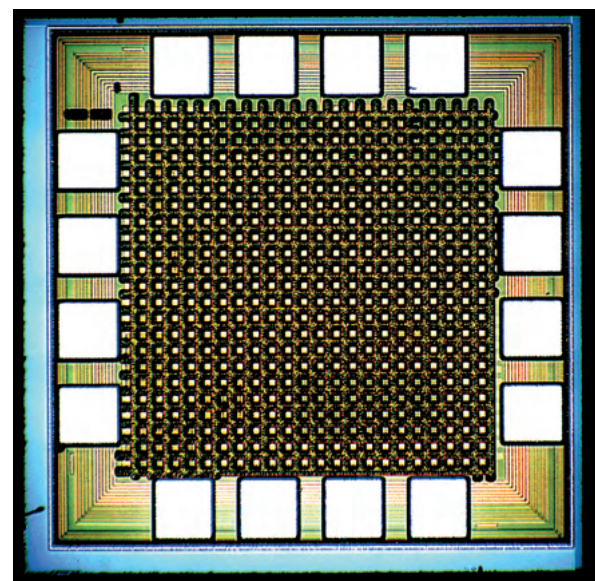|	
Contact:	Krzysztof Siwiec
E-mail:	K.Siwiec@chipcraft-ic.com
Technology:	GlobalFoundries 130nm SiGe 8XP
Die Size:	1.5mm x 1.5mm
Application Area:	Security / Privacy

Fig.1: Micrograph of the fabricated IC.

Introduction

The designed IC is the first step in the development of a miniature infrared detector module, where the detector and transimpedance amplifier are integrated into one package. The main challenge was to obtain low input referred current noise for wide range of detector impedance. It was achieved by exploiting possibilities of GF 130nm SiGe BiCMOS technology.

Description

The developed transimpedance amplifier was designed to achieve low input referred current noise for detector impedance from tens of Ohms, up to hundreds of thousands of Ohms. Depending on impedance value, the operational amplifier used in the transimpedance amplifier must have either low input referred voltage or current noise. Low input reference noise can be achieved using bipolar input stage, while low input referred current noise is achievable with MOS based input stage. To cover wide detector impedance range, input stage composed
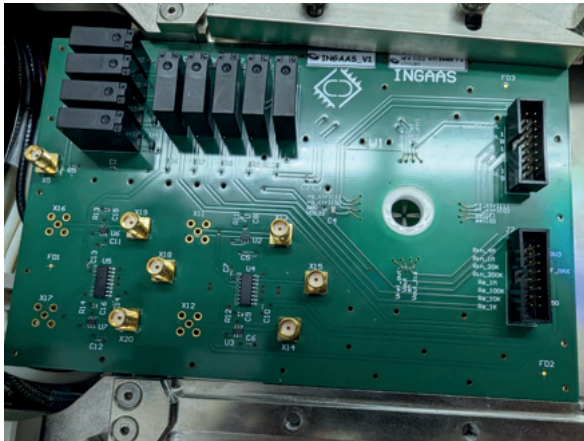
Fig.2: Probe card used for IC characterization.

of bipolar and MOS transistors has been used, where ratio between bipolar and MOS transistors usage is programmable. To make the IC flexible, the transimpedance of the amplifier is programmable. Additionally, the IC is equipped with a programmable voltage gain amplifier designed to drive 50 Ohm load. The chip also consists of voltage and current reference circuit and PTAT that allows to monitor the module temperature.

Results

Fabricated device (Figure 1) has been characterized using a dedicated probe card (Figure 2). The measurements results show that the design goals have been achieved and are in good alignment with simulation results. The amplifier achieved input referred voltage noise below 1 nV/sqrt(Hz) for low impedance detectors and input referred current noise below 0.2 pA/ sqrt(Hz) for high impedance detectors. Achieved results are state of the art.

Why EUROPRACTICE?

We have been working with EUROPRACTACE for several years. EUROPRACTICE offers MPW service in various technology nodes and variants for SMEs, together with professional support. It allowed us and our customers to develop several ASIC projects, some of which are already in volume production.

Radio receiver front-end at 300 GHz for 6G
CWC-RT, University of Oulu, Oulu, Finland

Contacts: Sumit Pratap Singh, Mostafa Nokandi, Mohammad Montaseri Timo Rahkonen, Marko E Leinonen and Aarno Pärssinen

E-mail: FirstName.LastName@oulu.fi

Technology: IHP 0.13µm SiGe BiCMOS SG13G2

Die Size: 2.14mm x 0.935mm

Design Tools: Cadence

Application Area: Datacom / Telecom

Introduction

Future generation of wireless communication, beyond-5G and 6G, would need ultra-high speed data rate of 100 Gbps to 1 Tbps. This would require 10s of GHz of radio bandwidth to support data-rate-intensive applications such as holographic communication, mixed reality etc. Sub-THz and THz frequency bands offer higher relative bandwidth as compared to mmWave frequency range. SiGe BiCMOS based semiconductor technologies, with maximum speed of oscillation of 450 GHz, offer high performance bipolar devices along with MOS devices to implement on-chip digital circuits. This provides a great opportunity to implement high performance and highly integrated RF transceivers at sub-THz/THz frequency ranges for ultra-high-speed communication. This design attempt mainly aims to implement radio front-end at 300 GHz band to support beyond 100 Gbps data rate of wireless communication.

Description

Figure 1 depicts the die micrograph of mixer-first sliding-IF receiver front-end implemented at 300 GHz band. This design is implemented using IHP's SiGe BiCMOS technology with ft/Fmax of 300 GHz/450 GHz. This receiver architecture downconverts the carrier signal in two steps. Firstly, carrier signal at 300 GHz is
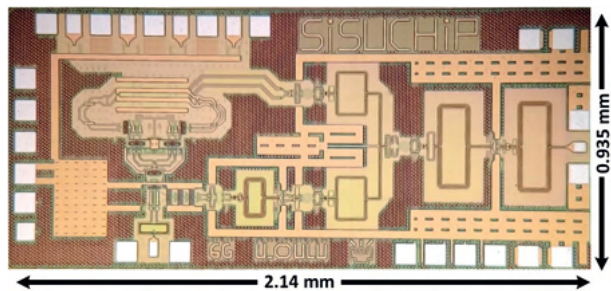

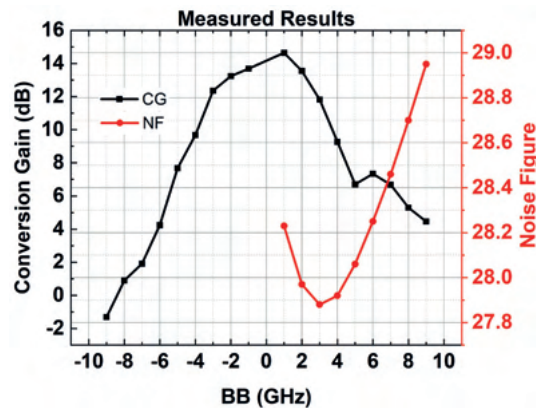Fig.1: Die micrograph of receiver front-end.

Fig.2: Measured baseband response and noise figure of the receiver front-end.

downconverted to 100 GHz IF with 200 GHz LO signal, and then, 100 GHz IF signal to 0-IF IQ signal by using 100 GHz IQ LO signal. LO signal, at two-third of carrier signal frequency, is generated by two cascaded frequency doubler and external LO signal of 50 GHz. First frequency doubler output at 100 GHz is used at IQ mixing branch. Quadrature LO signal at 100 GHz is generated by quadrature hybrid coupler (QHC) for 90-degree phase shift.

Results

Figure 2 shows the measured baseband response and noise figure of the receiver front-end. Measured peak gain is 15 dB with 3-dB/6-dB bandwidth of 8 GHz/12 GHz. Measured input-referred compression point (P1dB) is -17 dBm. Due to sliding-IF architecture, DC power consumption in this work is lowest among the SiGe BiCMOS based receivers. Despite operating close to maximum frequency of oscillation of semiconductor technology, this receiver front-end offers one of the best dynamic ranges in this category.

Why EUROPRACTICE?

One-stop solution and services by EUROPRACTICE have been quite satisfactory for ASIC design tape-outs. Our experience with the customer support team has also been pleasant.

Acknowledgements

This research work has been financially supported by the Academy of Finland 6G Flagship (grant 346208). We also would like to thank Keysight Technologies for measurement equipment donation.

References

Singh, S. P. et al. A 300-320 GHz Sliding-IF I/Q Receiver Front-End in 130 nm SiGe Technology. 2023 IEEE Radio Freq. Integr. Circuits Symp. (RFIC) 00, 37–40 (2023).

A 195GHz LNA with on-chip and area efficient temperature compensation circuit

Tecnun – University of Navarra, San Sebastian, Spain

Contacts:	A. Urain, D. del Rio, R. Torres, R. Berenguer
E-mails:	auraine@tecnun.es, ddelrio@ceit.es, rberenguer@tecnun.es
Technology:	IHP 0.13μm SiGe BiCMOS SG13G2
Die Size:	0.71mm x 0.77mm
Design Tools:	Cadence Virtuoso and Siemens Calibre
Application Area:	(Aero)Space

Introduction

Recent advances in Silicon-based CMOS and BiCMOS processes are opening the path for the development of Systems on Chip (SoC) to cover the high mmW and sub-THz frequency bands. SiGe HBTs are more extensively used for these purposes since they offer a superior gain, power and noise performance than their CMOS counterparts. The main drawback is that the HBT collector current varies exponentially with temperature, which makes it challenging to design mmW integrated circuits robust to the temperature variations that are required to comply with industrial standards. Working close to or above half the fT of the technology limits the maximum gain per stage, which prevents using compensation schemes that introduce penalty in the maximum achievable gain and which forces to move towards multistage topologies as the operating frequency increases. The consequence is that the gain degradation due to temperature variation of each stage is added and it results in an overall variation of more than 10dBs. This can completely jeopardize the performance of the system if not addressed correctly, making it compulsory to compensate for the effect in applications aiming at industrial or space operating conditions.

Description

A 3-stage single-ended cascode LNA centered around 195GHz has been designed. The nominal collector currents of each stage have been chosen to find a compromise between gain and NF. Transistor sizes are incremental with each stage to decrease the output reactance and, therefore, to have more relaxed interstage matching networks that are realized with custom designed MOM capacitors (0.19fF/μm). In order to boost the gain of the amplifier, the common base transistor sizes are
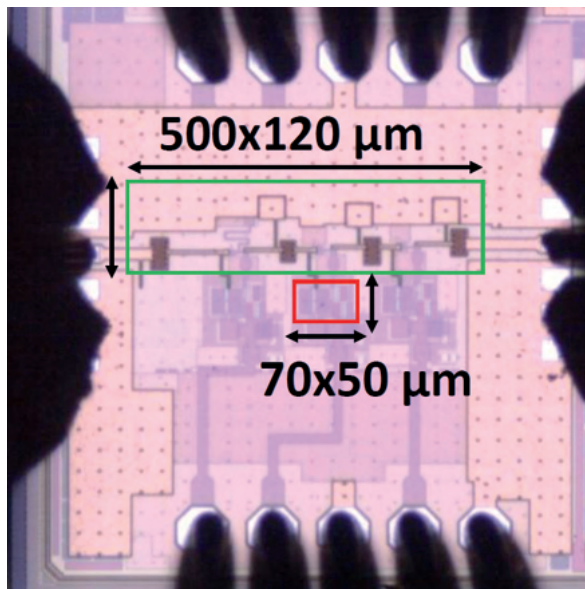
Fig.1: Chip micrograph (0.55mm²) with the core LNA (0.07 mm²) and the biasing circuits for each stage (0.0035mm²).

lower than the comment emitter ones, and noise cancelling is performed by introducing a shunt transmission line between transistors in the first stage. Finally, supply and ground planes are designed in an interleaved sandwich manner to increase the decoupling capacitance and minimize their impact.

The new proposed temperature compensation circuit achieves the desired PTAT current by introducing 4 resistors to the already needed biasing cascode current mirror.

The amplifier has been manufactured in the 0.13um SG13G2 technology offered by IHP, with ft/fmax=300/500GHz HBT transistors. The chip micrograph is shown in Figure 1, which occupies an overall area of 0.71mm x 0.77mm with pads.

Results
A temperature compensated 195GHz LNA has been designed, achieving a stable NF of 9dB (+/-1.5dB) and a stable gain of 18dB (+/-1.1dB) over a wide temperature range of at least -20°C to 80°C, thanks to on-chip and low area biasing circuit. The 3-dB bandwidth of the LNA is 25GHz. [1]

Why EUROPRACTICE?
TECNUN, the school of engineering of the University of Navarra, has been using EUROPRACTICE services for many years. EUROPRACTICE offers designers and researchers the opportunity to prototype their designs at an affordable price.

As well, EUROPRACTICE staff are very responsive and helpful, providing excellent technical support through the different stages of the tape-out.

Acknowledgements

References
[1] A. Urain, D. D. Río, R. Torres and R. Berenguer, "A G-Band SiGe BiCMOS LNA With an On-Chip and Compact Temperature Biasing Circuit" 2023 IEEE/MTT-S International Microwave Symposium – IMS 2023, San Diego, CA, USA, 2023, pp. 1132-1135.

An adjustable True Time Delay for D-Band beamforming applications

Friedrich-Alexander-Universtität Erlangen-Nürnberg, Germany

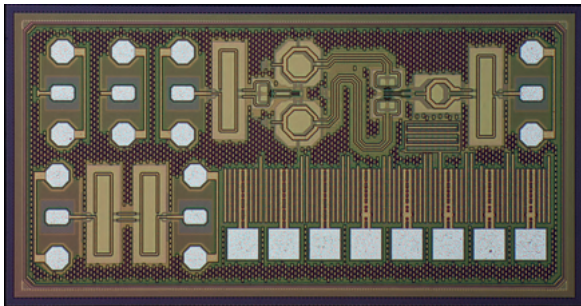|	
Contact:	Manuel Koch
E-mail:	manuel.koch@fau.de
Technology:	IHP 0.13μm SiGe BiCMOS SG13G2
Die Size:	1360μm x 690μm
Design Tools:	Cadence Virtuoso
Application Area:	Datacom / Telecom

Fig.1: Die Micrograph of the characterized True Time Delay circuit, with input being on the left and output on the right, together with calibration structures.

Introduction

Due to small antenna geometries and limited performance of semiconductor amplifiers at submillimeter frequencies and above, it is hard to maintain sufficient link budgets in communication and radar applications. An often-seen approach to compensate for these shortcomings is to employ antenna arrays with beamforming capabilities to improve the antenna gain. In order to control beams of these high data rate systems, analog circuits can avoid excessive computational effort arising from digital beamforming algorithms. However, commonly used phase shifters offer limited bandwidth due to beam squinting. Therefore, a True Time Delay architecture has been investigated.

Description

As the core working principle, the designed chip uses the delay-sum approach. The core idea is to split the incoming RF signal into two parts, which are offset by a relative time delay. A variable time delay is realized when the signals are combined using an adjustable ratio. In order to achieve the targeted true time delay, a delay line is used as core delay element, which also defines the tuning range.

In theory, a time delay of up to 90°, at the targeted maximum frequency, can be realized if moderate signal distortion is accepted.

The presented chip implements this technique by using a digitally controlled power splitter, a delay line of 90° at 140 GHz and a power combining amplifier stage. All three stages can be clearly identified in Figure 1. The power splitter and all bias currents are controlled by onchip DACs via an SPI interface. The bias currents can also be used to compensate for gain variation.

Results

The test structure has been characterized on-chip and shows a continuously tuneable delay range of 1.75ps at 144 GHz center frequency with 18% bandwidth, limited by the amplitude response. It achieves a gain of 0dB with a variation of 0.5dB across its tuning range by a very simple compensation scheme using the bias currents.

While the available delay range is not sufficient for delaying individual antennas in large arrays it can be used for steering the angle of 2x1 or 2x2 subarrays. To the best of the authors knowledge, the presented delay element uniquely offers the feature of a continuously tuneable time delay in the demonstrated frequency range. Offering this property, it is able to significantly reduce the area of switched delay line True Time Delays, as sub-millimeter wave switches often require $\lambda/4$ transmission lines.

Why EUROPRACTICE?

For us, the uncomplicated and reliable access to several state-of-the-art semiconductor processes is a very valuable service, especially due to the always helpful support by EUROPRACTICE, when difficulties or questions arise. Likewise, the access to a variety of EDA tools is crucial for teaching and research at our institute.

Acknowledgements

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SiGe 27-GHz Cascode Doherty Power Amplifier

Institute for Applied Microelectronics (IUMA), Canary Islands, Spain

Contact:	Victoria Díez Acereda
E-mail:	vdiez@iuma.ulpgc.es
Technology:	IHP 0.13µm SiGe BiCMOS SG13S
Die Size:	1.73mm x 1.73mm
Design Tools:	Cadence Virtuoso
Application Area:	Datacom / Telecom

Introduction

The Doherty Power Amplifier (DPA) operates in the K-band and is designed for 5G wireless communications at 27 GHz. We designed this amplifier as part of the GANTECH (Design of GaN Power Amplifiers for Communications) project. The goal of this project is to improve the efficiency of power amplifiers, particularly at back-off levels, while reducing area.

Description

Two versions of the DPA were fabricated. The first version uses inductors provided by the foundry and the second version employs user custom solenoid inductors, reducing the circuit area. Both circuits employ an asymmetric configuration where the auxiliary amplifier is larger than the main amplifier. The main amplifier operates in class-AB, and the auxiliary in class-C. Additionally, both circuits draw a total current of 22 mA from a 3.3 V DC power supply.

Results

The first version of the DPA achieves a maximum PAE of 23.2%, providing 25dBm of output power. At 9dB of back-off, the efficiency decreases to 18%. This circuit size is 1.48mm x 0.98mm, including pads.

The second version of DPA achieves a maximum PAE of 17.2%, delivering 23dBm of output power. At 9dB of back-off, the efficiency remains at 16%. The circuit size is 1.43mm x 0.73mm, including pads and its area is lower than the one designed with the Process Design Kit (PDK) inductors due to the use of custom made solenoid inductors.

Why EUROPRACTICE?

We chose EUROPRACTICE because they provide access to cutting-edge technologies and support for GDSII submission procedures. Furthermore, EUROPRACTICE offers comprehensive
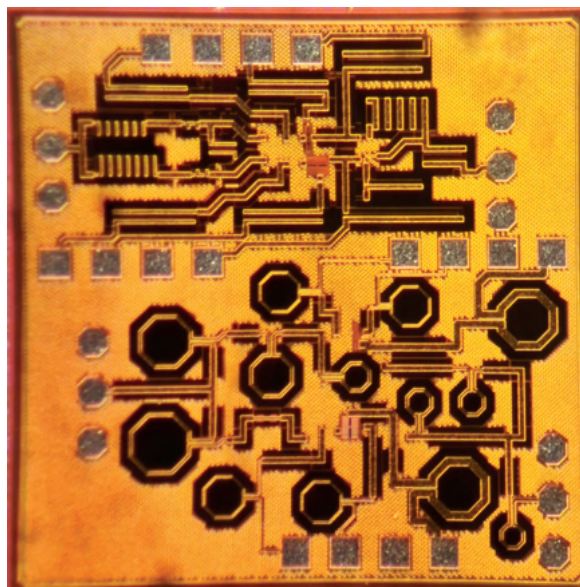

Fig.1: Microphotograph of two Doherty Power Amplifiers: the amplifier using custom made solenoid inductors (top), the amplifier using PDK inductors (bottom).

prototyping, packaging, and testing services for state-of-the-art technologies with mature PDKs at reasonable prices. Without these services, our ability to take innovative projects or conduct advanced research would be severely limited.

Acknowledgements

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Harmonic Rejection N-Path Mixer for Low Power Applications
TIMA Laboratory, Grenoble INP, Grenoble, France

Contacts:	Sana Ibraim, Serge Subias, Florence Podevin, Laurent Fesquet, Sylvain Bourdel
E-mail:	sana.ibrahim@univ-grenoble-alpes.fr
Technology:	ST 28nm FD-SOI CMOS
Die Size:	1585µm x 1094µm
Design Tools:	Cadence Virtuoso
Application Area:	IoT

Introduction

Parallel radio reception is the capability of a radio receiver to simultaneously process multiple radio signals on different frequencies or channels. This is achieved through the use of multiple radio frequency (RF) front ends or tuners, each tuned to a specific frequency and connected to a separate demodulator. This architecture is applied in various fields, such as multi-channel radio receivers, cellular base stations, and satellite communications, enabling efficient use of the radio spectrum without interference. However, N-path mixers, particularly harmonic rejection N-path mixers (HR-NPM), play a crucial role in parallel radio reception systems by facilitating simultaneous reception of multiple signals while suppressing unwanted harmonic frequencies that can cause interference and degrade performance. The proposed mixer features a wide bandwidth RF front-end suitable for low-power multi-standard receivers while keeping low complexity where it can reject up to the 6th harmonic included.

Description

The designed chip is fabricated in 28nm CMOS28FDSOI technology from ST, and it includes two main designs: the first one is the low noise amplifier LNA standalone, so it can be possible to measure this latter alone and to provide the required matching, gain and NF by this block. The second design is the front-end design including the LNA, mixer, voltage-controlled oscillator VCO and an output buffer. Designing a front-end receiver involves addressing numerous challenges within each component of the chain. The LNA, the initial active stage following the antenna, presents challenges such as achieving high gain, low noise figure, adequate linearity, minimized power consumption, and optimized input/output matching.
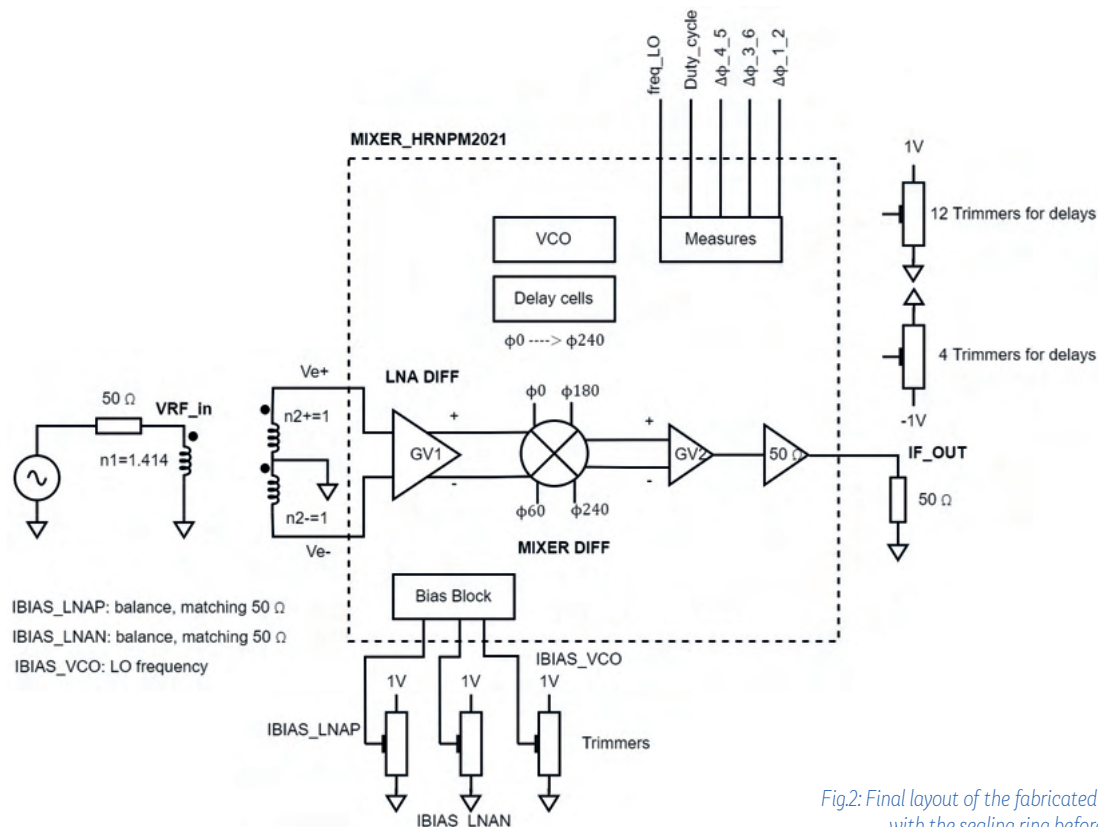

Fig.2: Final layout of the fabricated circuit with the sealing ring before tiling.
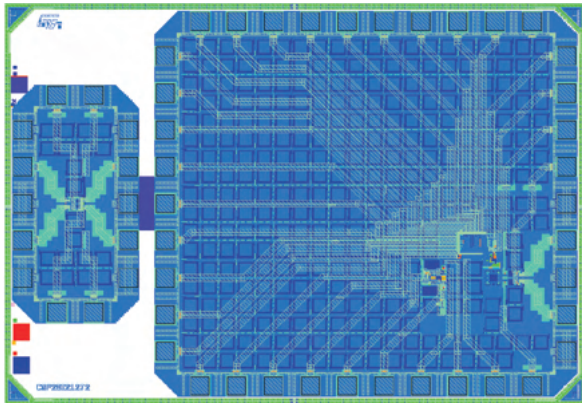
Fig.1: Block diagram of the RF front-end for the implemented HR-NPM.

The subsequent block, the mixer, often employs passive mixers with a primary challenge being the attainment of sufficient conversion gain while maintaining low noise figure and addressing inherent nonlinearity to prevent signal distortion and unwanted spurious signals. The mixer is controlled by a VCO, which introduces challenges such as achieving a wide frequency tuning range, minimizing phase noise, reducing power consumption, and ensuring accurate signals with precise delay and duty cycle. The latter challenge is particularly critical and stands out as the most important aspect of the entire design process.

Results

The circuit has been received recently and has yet to be tested.

Why EUROPRACTICE?

Grenoble INP has been using the EUROPRACTICE services via CIME-P (former CMP) for several years. This choice is driven by the opportunity they provide to manufacture circuits using STMicroelectronics technologies, in this case, FDSOI 28nm.

References

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[3] A. Al Shakoush, E. Lauga-Larroz, F. Podevin, S. Ibrahim, L. Fesquet, S. Bourdel, "Improved pi-delayed harmonic rejection N-path mixer for low power consumption and multistandard receiver," in 2022 20th IEEE Interregional NEWCAS Conference (NEWCAS), IEEE, 2022, pp. 170-173.

Ultra-high resolution mm-wave phase shifters in 28nm FDSOI

Cornell University, Ithaca, NY, USA

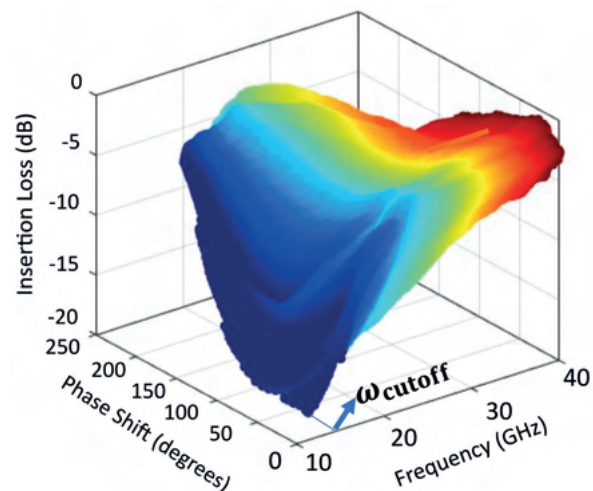|	
Contacts:	Bal Govind, Thomas Tapen, Alyssa Apsel
E-mail:	bg373@cornell.edu, aba25@cornell.edu, tpt26@cornell.edu
Technology:	ST 28nm FD-SOI CMOS
Die Size:	0.177mm x 0.367mm
Application Area:	Datacom / Telecom

Fig.1: Measured tuning characteristics for 4096 states of the digitally tuned 20-35 GHz phase shifter, in terms of insertion loss and phase vs frequency.

Introduction

This device solves a fundamental problem in beam steering of 5G MIMO signals in the 20 to 40 GHz band. It breaks the loss vs. resolution trade-off and achieves 0.2 degrees of phase tuning with under 7dB of loss (two orders of magnitude higher resolution, with low loss) while being completely passive. Therefore, it is an ideal candidate for phased arrays, sub-wavelength metasurfaces, passive radar and coupled oscillators.

Description

We designed tunable loaded transmission lines and capacitor banks using low Vt RF NFETs in the 28nm FDSOI process. We coiled up these lines and exploited multiple LC resonances to form highly reflective loads in a reflective type phase shifter structure. Key to the compact nature of our phase shifter is the microwave hybrid coupler that is built with overlapping inductors on two RF metal layers, with ultra-broad bandwidth.
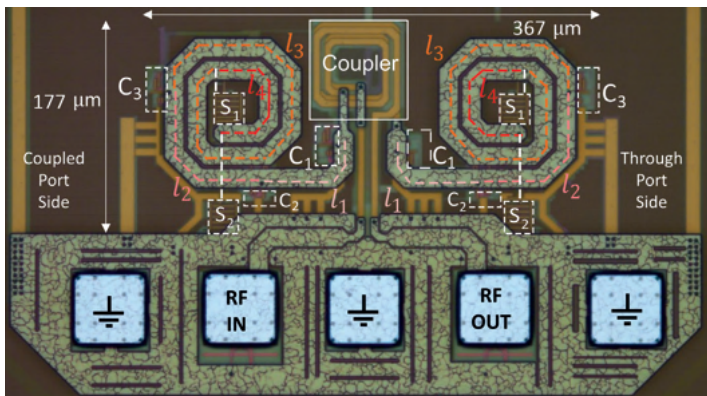
Fig.2: Chip photograph showing the ultra-compact reflective transmission lines used in combination with the microwave coupler. Each transmission line consists of a distributed structure of mutual inductances and five-bit capacitor banks inserted intermittently.

This version has twelve bits of tunability, with options to bring portions of the lines in and out action through switches (MACROMOS RF devices).

Results

We have measured excellent insertion loss vs frequency metrics above 20 GHz, with over 230 degrees of phase shift. This device can be cascaded to extend beyond 360 degrees without added loss. It can be used as a unit cell in phased array in a sub-wavelength form factor. This would help boost the array factor since it can be integrated densely. This would mean sharp directivity of 5G radio communication to cell phones and base stations and suppressed sidelobes in the beams because of extremely sharp resolution.

Why EUROPRACTICE?

We have received good support from a EUROPRACTICE partner CIME-P in chip fabrication and packaging.

Acknowledgements

We thank STMicroelectronics (Andreia Cathelin), CIME-P and EUROPRACTICE for supporting several of our MIMO component tapeouts.

References

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Solving Combinatorial Optimization Problems using coupled Oscillators
Technical University of Darmstadt, Darmstadt, Germany

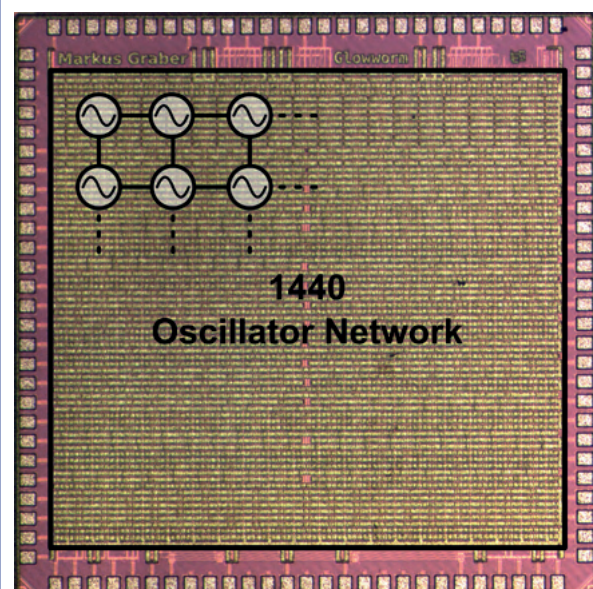|	
Contacts:	Markus Graber, Klaus Hofmann
E-mail:	Klaus.Hofmann@ies.tu-darmstadt.de
Technology:	TSMC 28nm HPC+
Die Size:	2.1mm x 2.1mm
Design Tools:	Cadence Virtuoso, Cadence Innovus, Siemens Calibre, Synopsys Design Vision
Application Area:	High Performance Computing (HPC)

Fig.1: Die shot of the 1440 oscillator system.

Introduction

Solving combinatorial optimization problems is a common task in virtually all areas of modern life. It is not only relevant in science, engineering, and technology, but for example also needed for scheduling flight plans, production, or transportation. Unfortunately, such problems are often NP-hard. This means, that no algorithm can solve such problems within a polynomial increasing runtime. In practice, the computational effort explodes making those problems especially difficult to solve. The needed runtime to solve such problems increases exponentially with the problem size. Despite continuous advances in digital processors, classical computing approaches cannot deliver the desired performance in terms of speed and energy efficiency.
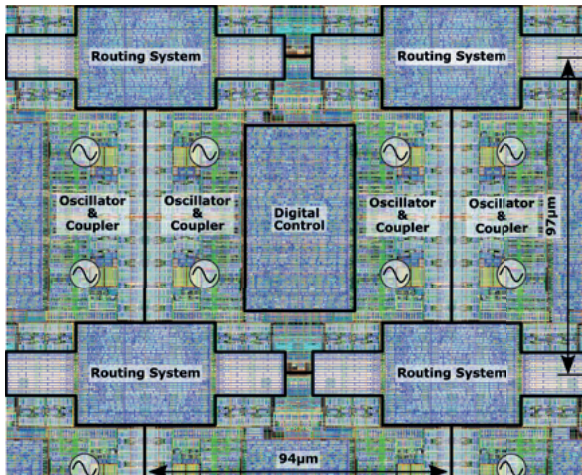
Fig.2: Layout view of the tiles containing the oscillators, including their couplers, digital control and routing system.

However, directly exploiting the natural analog behavior can lead to serious advantages. The approach of so-called Oscillator-based Ising Machines directly exploits the analog coupling dynamics between oscillators for computation in the phase domain.

Description

Our chip consists of a configurable network of 1440 ring oscillators. They are implemented as 4-stage differential architecture to be robust against power supply variations and noise. A total of 11,724 configurable coupler circuits, which can be set to different strengths using DACs, enable interaction between specific oscillators on demand. A routing system allows for flexible connections between arbitrary oscillators on the chip. So, an optimization problem is directly represented in the configurable hardware. When running, the oscillators manipulate each other's phases and naturally strive towards a (local) minimum state. This phase-state is measured by a phase-to-digital converter, which directly forms the solution of the optimization problem. The backbone of this system forms a digital configuration and control block. It manages the configuration and takes care of the communication with an external host system. Similar to FPGAs, the circuit blocks are organized in tiles, which are replicated to form the whole network. Furthermore, multiple calibration schemes are used since device mismatch and PVT variations are major challenges for any analog design in modern technology nodes. A frequency, a phase, and a delay calibration scheme effectively compensate for such variations.

Results

Our oscillator-based Ising machine solves optimization problems within just 950ns at a power consumption of less than 460mW. For comparison purposes, computing the reference solution on a 24-core workstation took on average 8 orders of magnitude longer with roughly 3 orders of magnitude higher power consumption. However, it could guarantee that the found solution was optimal. The solutions are very close to the best-known solution across hundreds of tested benchmark problems. It reaches at least 94% of the best-known solution on average and typically even more. However, this computing system does not find the best-known solution and can give no guarantee. The computation itself is strictly non-deterministic due to the inherent noise and the chaotic response of the oscillator computing principle.

Why EUROPRACTICE?

EUROPRACTICE offers a flexible and affordable opportunity to tape out the design. The flexible sizing options in 0.1mm² steps allow us to just use as much area as we need for our design. The EUROPRACTICE service gives uncomplicated, quick, and helpful advice for any tape-out-related issues.

Acknowledgements

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A 1.8V GPIO designed with only core transistors for sub-3nm GAA technology

imec, Leuven, Belgium

Contacts:	Wen-Chieh Chen, Mang-Ching Huang, Shih-Hung Chen
E-mail:	wen.chieh.chen@imec.be
Technology:	TSMC 28nm HPC+
Die Size:	1mm x 1mm
Design Tools:	Cadence
Application Area:	IoT

Description

We have demonstrated the output stage in previous chips. In this tapeout, we focus on the innovative design of input stage of the proposed I/O interface. The new flow of input stage consists of a dynamic-gate-bias circuit, a hysteresis control circuit, a level-down shifter and an input buffer, as shown in Figure 1. The proposed dynamic-gate-bias circuit generates required signal in the VDD/2VDD domain depending on the received I/O signal. The proposed level-down shifter not only decreases the voltage level to core domain but also ensures that the duty cycle follows the received I/O signal, providing

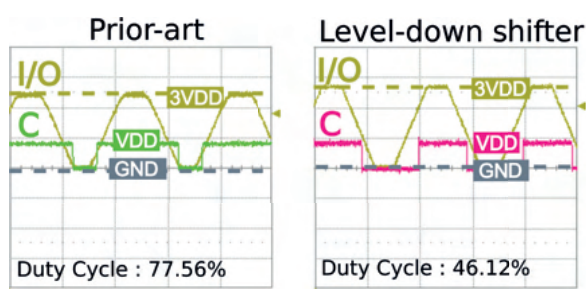Fig.1: The flow chart of the proposed input stage.

Fig.2: Measurement results of two voltage-lowering techniques of prior art and the proposed level-down shifter.

an advantage over the prior art. This input stage flow can also enable hysteresis function by a Schmitt trigger independently without being impacted by other circuits.

Results

The input stage can successfully receive a 3xVDD signal and transfer it to a VDD signal. Compared to the prior art voltage-lowering technique, the level-down shifter can improve the duty cycle from 77.6% to 46.12%, as shown in Figure 2. The hysteresis window can achieve 24%VDDIO.

Introduction

Semiconductor industry has been pursuing logic dimensional and structural scaling for better power-performance-area-cost (PPAC). As we are entering gate-all-around (GAA) scaling era, the gate accommodation issue comes to I/O transistor fabrication. The dense nano-sheet (NS) pitch is too narrow to accommodate I/O-gate-stack layers. The gate metal has no room to fill in after thick-oxide and high-K layer deposition. However, for an I/O interface circuit, it usually requires I/O transistors to communicate effectively between cores and the external world without reliability issues. Thus, we proposed a pure circuit solution to the gate accommodation issue of I/O transistor fabrication in GAA-NS technology. It is a high-voltage tolerant bi-directional general-purpose I/O (GPIO) which can tolerate 3xVDD and only consists of core transistors. This chip is mainly designed for functional demonstration of our proposed GPIO.

Why EUROPRACTICE?

Thanks to EUROPRACTICE providing affordable tapeout chances, dedicated CAD tool licences, and supportive technical assistance, we successfully have had series of tapeouts for this GPIO development over the past several years. This year we joined a mini@sic January 2023 tapeout in the TSMC 28nm technology and validated our idea with Si proof.

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Ultra-Fast Single Photon Counting ASIC for Fast Synchrotron Applications

AGH University, Cracow, Poland – European Synchrotron Radiation Facility (ESRF), Grenoble, France

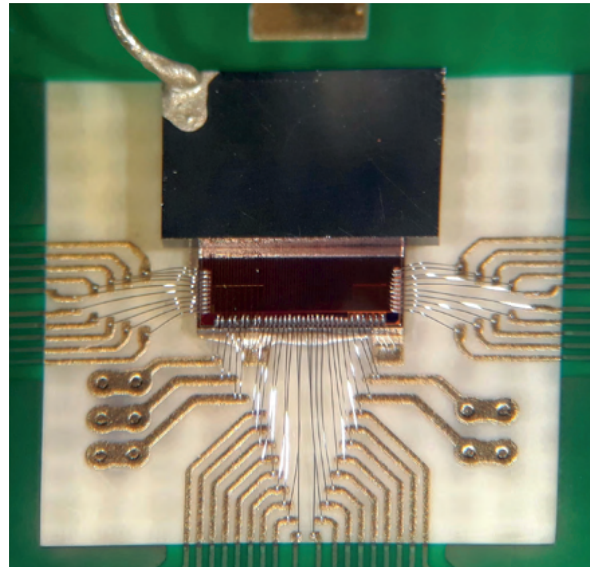|	
Contact:	P. Kmon
E-mail:	kmon@agh.edu.pl
Technology:	TSMC 40nm GP
Die Size:	3.2mm x 3.5mm
Design Tools:	Cadence Virtuoso, Spectre, Siemens Calibre
Application Area:	X-ray Imaging

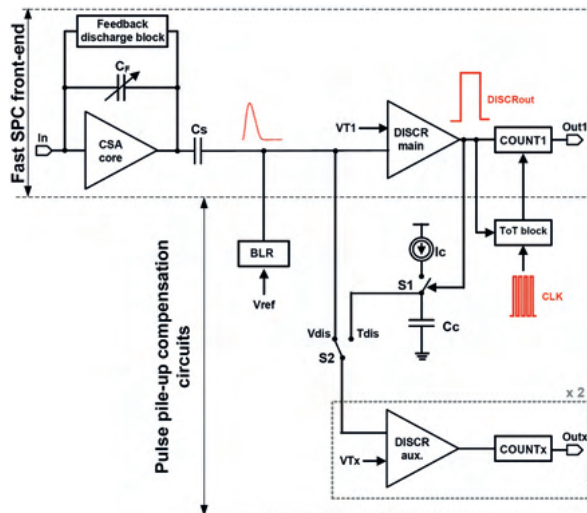Fig.2: Chip photo with mounted detector.

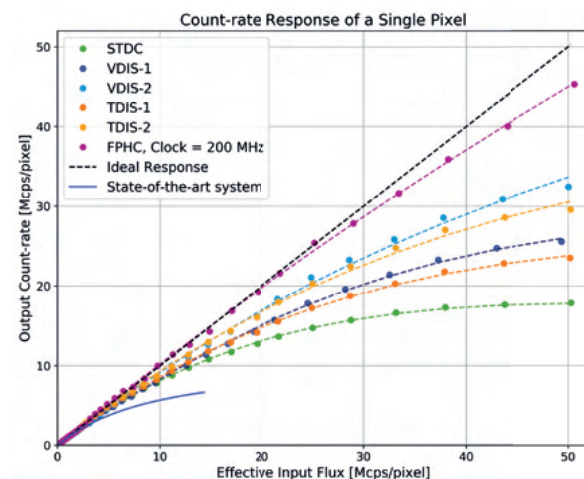Fig.1: Schematic idea of the recording channel.

Fig.3: Count-rate curves for different chip operating modes.

Introduction

The main motivation of the project was to propose an integrated solution that could target a new generation of photon counting hybrid pixel detectors for synchrotron radiation applications with small pixels. Therefore, we decided to use the modern TSMC 40nm process that allows the implementation mixed-mode integrated circuits.

Description

The SPHIRD (Small Pixel High Rate photon counting Detector) project is an R&D study to investigate how far the photon counting X-ray hybrid pixel detector technology can go, regarding photon rate and spatial resolution. A goal was to boost by 30 times the count-rate capabilities of existing detectors of similar pixel size. SPHIRD targets that figure by designing fast front-end electronics, by including pile-up compensation techniques in the pixel logic, and by implementing smaller pixels.

Each pixel contains fast front-end analog electronics (pulse width is only 18ns) with base-line holder (BLH), a set of discriminators (with offset trimming blocks), ripple counters, and digital blocks. The pixel architecture allows also for operation in conventional mode (STDC) and with different pulse pile-up compensation methods (these are voltage and time based methods named VDIS, TDIS, and FPHC respectively).

Results

We have managed to design, send to fabrication, and perform measurements of the 2048-channels integrated circuit dedicated to photon counting detectors. The measurements with an X-ray beam performed at bending magnet beamline in the European Synchrotron Radiation Facility in Grenoble showed that the chip's count-rate performance exceeds largely currently existing detectors. This has been achieved mainly thanks to the special readout features implemented in SPHIRD, the pile-up compensation methods, the pixel relocation algorithms, and TSMC 40nm process used.

Additionally, the on-chip pixel relocation techniques reduce the photon losses at the pixel corners opening the door to the implementation of detectors with pixel pitch smaller than 50 μm. Importantly, moving to smaller pixels will not only increase the intrinsic spatial resolution of the detector, but also allow to better exploit the subpixel relocation modes.

Why EUROPRACTICE?

AGH University has benefited from the EUROPRACTICE offer for many years, with a lot of successful tapeouts. EUROPRACTICE offers affordable fabrication of our prototypes in MPWs and mini@sics and provides access to a wide variety of design tools. It is an essential partner in our research.

Acknowledgements

The chip design was realized by P. Grybos, R. Kleczek, P. Otfinowski, and P. Kmon (AGH UST) while synchrotron experiments were conducted by P. Fajarado, D. Magalhaes, and M. Raut.

References

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HEEPocrates: An Ultra-Low-Power RISC-V Microcontroller for Edge-Computing Healthcare Applications
Embedded Systems Laboratory (ESL), EPFL, Lausanne, Switzerland

Contacts: Simone Machetti, Pasquale Davide Schiavone, Thomas Christoph Müller, Alexandre Levisse, Miguel Peón-Quirós and David Atienza

E-mail: simone.machetti@epfl.ch

Technology: TSMC 65nm LP MS/RF

Die Size: 2mm x 3mm

Design Tools: Siemens Questasim, Synopsys Design Compiler, Cadence Innovus

Application Area: Healthcare

Introduction

The field of edge computing in healthcare has seen remarkable growth due to the increasing demand for real-time processing of data in applications. However, challenges persist due to limitations in healthcare devices' performance and power efficiency. To overcome these challenges, heterogeneous architectures that combine host processors with specialized accelerators have emerged, leading to improved performance and power consumption.

In this work, we present HEEPocrates, an ultra-low-power RISC-V microcontroller for edge computing healthcare applications. The chip combines the open-source eXtendible Heterogeneous Energy-Efficient Platform (X-HEEP) [6] with a coarse-grained reconfigurable array (CGRA)[3] and in-memory computing (IMC) [7] accelerators, both of which are efficient in reducing the energy consumption of healthcare applications [2].

Description

Figure 1 shows the HEEPocrates architecture and how the CGRA [3] and IMC [7] accelerators are integrated.

The X-HEEP host platform [6] is configured with:

1) a CV32E20 core [5], which is optimal for running control tasks and offloading performance-intensive computations to the external accelerators;

2) 8 SRAM banks of 32 KiB to accommodate variable lengths of data while power-gating the unused banks;

3) a fully connected bus to provide high-bandwidth capabilities to the CGRA [3];

4) all the available peripherals in place to deliver high flexibility;

5) a CGRA [3] and IMC [7] accelerators connected to the external eXtendible Accelerator InterFace (XAIF).
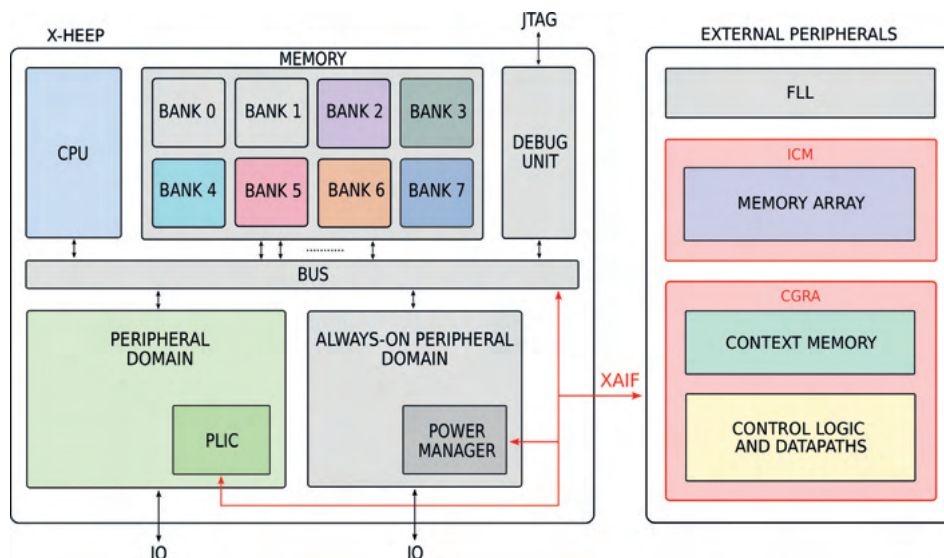
Fig.1: HEEPocrates
architecture.
Power domains are visually
marked using different
colors.
The components highlighted
in grey are always on.
The accelerator integration
is marked in red.

The design includes 11 power domains, marked with different colors, which can be independently clock-gated or power-gated when unused to reduce power consumption. Memory banks can also be set in retention mode.

Results

Figure 2 shows the HEEPocrates layout, the silicon photo, and the physical realization. The chip has been tested from 0.8 V to 1.2 V, achieving a maximum frequency of 170 MHz and 470 MHz, respectively. The power consumption ranges from 270 µW in 32 kHz and 0.8 V, to 48 mW at 470 MHz and 1.2 V.

To validate the design, we measured the energy consumption of healthcare applications running on the host CPU of HEEPocrates and on state-of-the-art microcontrollers commonly adopted in this application domain.

The selected microcontrollers cover the spectrum of ultra-low-power edge devices, ranging from top-tier power efficiency, with Apollo 3 Blue, to top-tier performance, with GAP9. Similarly, the benchmark covers the spectrum of ultra-low-power healthcare applications, ranging from acquisition-dominated, with heartbeat classifier [1], to processing-dominated, with CNN for seizure detection [4].

We have measured each application phase at each microcontroller's optimal frequency and voltage configuration. For HEEPocrates, we have run acquisition phases at 1 MHz, 0.8 V to reduce power while offering enough performance to acquire bio-signals in the order of hundreds of Hertz, and processing phases at the maximum speed of 170 MHz, 0.8 V to minimize processing time and race to sleep.

Figure 3 shows the energy alignment of HEEPocrates with the selected microcontrollers for both computationally hungry and acquisition-dominated healthcare applications. This demonstrates the real-world suitability of the chip for this application domain, known for its strict power and performance constraints.
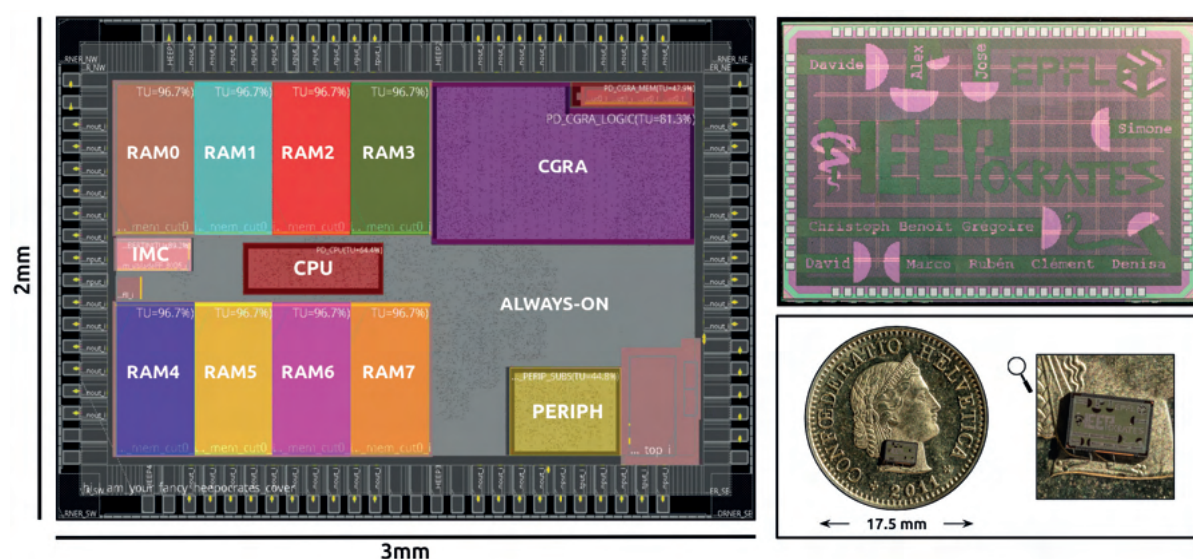

Fig.2: HEEPocrates layout, silicon photo, and physical realization (on a Swiss 5-cent franc coin).
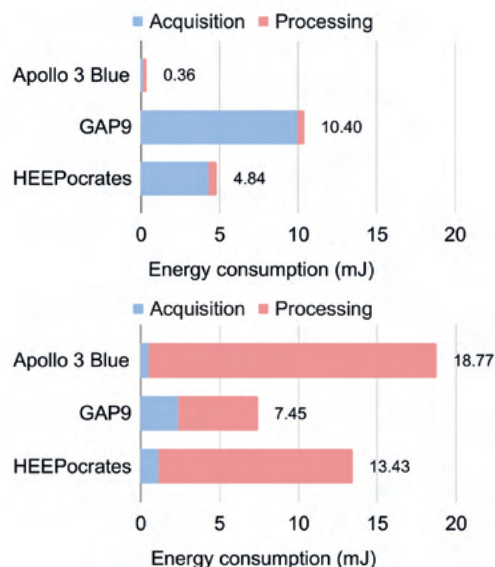
Fig.3: Energy consumption of the benchmark
running on relevant healthcare microcontrollers and on HEEPocrates.
(a) Heartbeat Classifier. (b) Seazure Detection CNN.

Why EUROPRACTICE?

EUROPRACTICE support is a key element in the success of this project. Their assistance in acquiring EDA tool licenses, access to technology design kits, participation in their mini@sic MPW program, and the design support from their team, which addresses all sorts of tricky questions, are extremely valuable for universities. Having such a partner is a great asset for EPFL, enabling high-quality research on systems-on-chips (SoC).

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PicoTDC: 64 channels Time to Digital Converter with ps time resolution
CERN, Geneva, Switzerland

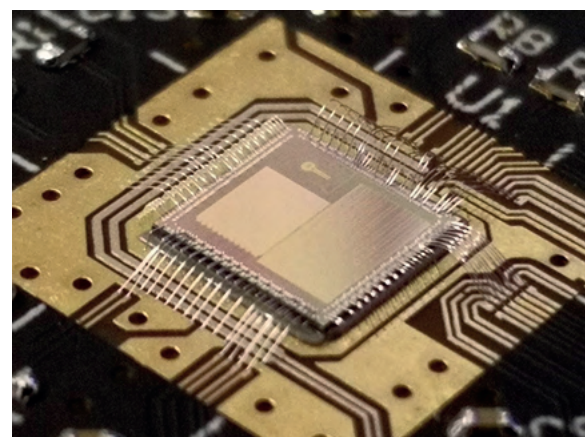|	
Contacts:	Moritz Horstmann, Jorgen Christiansen, Jeffrey Prinzie
E-mail:	Jorgen.christiansen@cern.ch
Technology:	TSMC 65nm
Die size:	5mm x 5mm
Design Tools:	Cadence design tools
Application Area:	High Energy Physics (HEP)

Fig.1: PicoTDC directly wirebonded to test board.

Introduction

The HEP community has an increasing need for very high time resolution measurements on a large number of channels for Time Of Flight (TOF) detectors and similar applications. The PicoTDC chip has therefore been developed as a successor of a previous TDC (named HPTDC), extensively used in the HEP community during the last 15 years.

Description

The PicoTDC is a 64 channel Time to Digital Converter (TDC) ASIC that can measure the time of digital signals with a time binning of 3ps or 12ps. Digitized timing of leading and/or trailing edges can be buffered on chip and also have the possibility to be filtered based on a trigger with configurable latency and time window.

The time of signal edges are measured relative to an input reference clock of 40MHz and digitized using on a very low jitter 1.28GHz PLL (Phase Locked Loop) followed by a time interpolator DLL (Delay Locked Loop), getting to a final timing binning of 3/12ps. Measurements are encoded to contain timing information of leading edge and/or trailing edge or alternatively
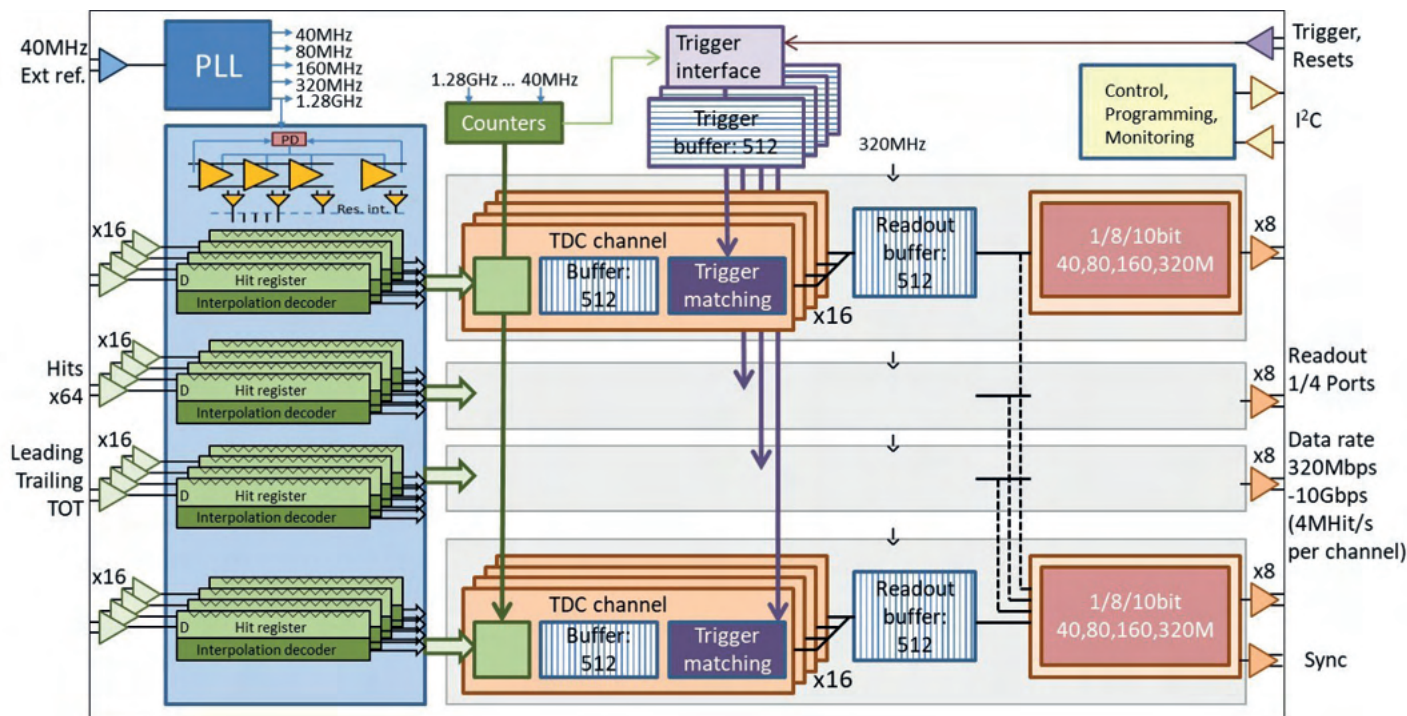
Fig.2: Architecture of 64 channel PicoTDC with extensive buffering and filtering capabilities.

as a leading edge together with pulse width for Time Over Threshold (TOT) measurements. Encoded time measurements are on each channel buffered in a 512 deep FIFO followed by an optional programmable trigger filtering window. Extracted hits from 4 channel groups, of 16 channels each, are merged into 512 deep readout FIFOs to four byte-wise readout ports at 320MHz. An external programmable timing calibration pulse signal can be generated by the chip with 3ps resolution.

Results

The final chip was submitted in 2019 and has been extensively tested for functionality and timing performance. All programmable digitization, buffering, triggering and readout options have been tested to be fully functional. Timing characterization has confirmed its excellent timing performance over its full dynamic range of 205us on all 64 channels. Effective single shot time resolution of 3.75ps RMS has been measured and as low as 1.35ps using an on-chip feature to correct for INL deviations.

PicoTDC chips are now available in quantity to the HEP and science community in a 400 pin BGA package. A starter kit, consisting of a PicoTDC board with FMC connector to an FPGA evaluation board, supplied with basic FPGA firmware and Python DAQ software has also been made available to interested users.

Why EUROPRACTICE?

EUROPRACTICE design tools have allowed students and young engineers to contribute effectively to the successful design and test of this very well working high performance TDC chip for use in scientific instrumentation.

The development of such complex ASICs requires the use of state-of-the-art EDA software tools for the design, implementation, and verification, both at the component level and the system level. EUROPRACTICE software service is an indispensable element for the ASIC developments at CERN and its collaborating institutes, supporting the use of a multitude of state-of-the-art EDA tools and facilitating coherency in the collaborating design framework of distributed design teams.

Custom microelectronics components implemented in advanced technologies are vital parts of today's complex scientific instruments. The services provided by EUROPRACTICE allow a large community of physicists and engineers at CERN and in tens of collaborating Institutes working on these projects to use state-of-the-art EDA software tools and access to advanced CMOS processes for the construction of unique scientific instruments with centralized high-quality technical support.

Reference

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CMOS based gas and liquid sensor
III-V Technologies GmbH, Vienna, Austria

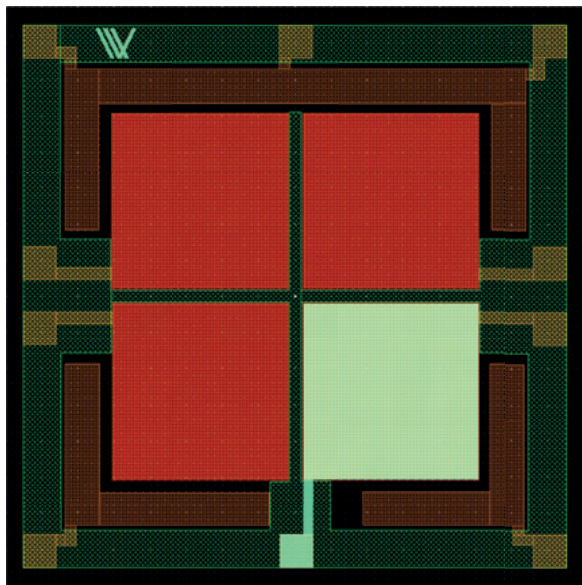|	
Contact:	Farshid Raissi
E-mail:	Raissi@iiivtech.com
Technology:	UMC L180 MM/RF
Die Size:	2.5mm x 2.5mm
Application Area:	Multi-purpose sensing

Fig.1: The mask layouts prepared for UMC's 180nm process. Two metal, polysilicon, n+ and field oxide layers are shown.

Introduction

III-V Technologies - SeTePa is a Vienna, Austria, based startup which focuses on disruptive approaches to semiconductor manufacturing. One idea pursued by SeTePa is the use of porous silicon to build sensors based on the single-electron effect. This effect provides the ability to measure tiniest changes in the dipole moment of its environment. This allows distinguishing of gases and liquids, and many could even be identified through this phenomenon. Applications for affordable, small devices built on this are endless, and the oil & gas industry is one of the markets SeTePa wants to work for.

While our porous samples have demonstrated excellent performance as gas and liquid sensors, we conceived an innovative approach to create a similar single-electron based sensor through contemporary CMOS technology. The prospect of manufacturing this sensor with CMOS presents numerous advantages, including cost-effectiveness, compact size, reproducibility, and the added benefit of seamless integration with electrical circuits. The technical concept is a large array of
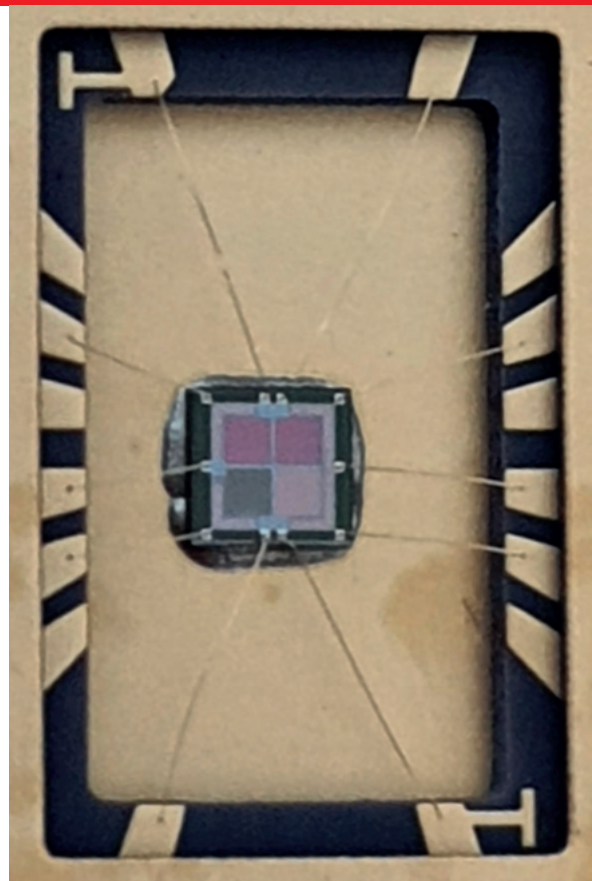

Fig.2: The sensors have been bonded to an open package for gas to be able to reach the sensors.

nano-sized single-electron elements that make up a robust sensor of a few square mm which can operate at room temperature (while many available gas detecting sensors require heating to high temperatures). The challenge was to produce samples of these elements using CMOS technology which would show the same behaviour as older prototypes based on porous silicon.

Description

Building the prototype: The n-well area used in the 180nm UMC process has the doping level necessary for obtaining the elements that exhibit single-electron effect. Polysilicon layer layout was used to define the shape and size of the elements. A network of more than one million 200nm by 200nm single-electron elements were produced for each sensor. In total, 4 individual samples were included in each die. One was used for temperature compensation; another was a single-electron transistor with a gate to modulate the IV and the two others were two actual sensors. The device used for temperature compensation was covered by insulation layers to prevent gas or liquid from touching its surface. The single-electron transistor is to be used later as a prototype for possible DC current standards.

Results

Preliminary results are outstanding. Aside from exhibiting single-electron effect at room temperature, the sensors

showed sensitivity to liquids as well as gases like CO_2, as expected. The actual measured results for CO_2 sensing are included in the figures. Measurement with different gases and liquids will continue to calibrate the samples and to produce a data sheet as this sensor has already garnered attention of external partners with specific requirements.

The result allows SeTePa to offer this sensing technology for integration. Now that standard CMOS can be used to manufacture the sensor arrays, the company can work on integrated devices which include other elements.

Why EUROPRACTICE?

For a fabless startup with a great technology portfolio but limited funding, EUROPRACTICE is a great way to get samples through multi-project wafers within a reasonable amount of time. We could not have been more pleased and appreciative of the help we got from EUROPRACTICE and its employees. When we encountered issues with design or design rules, interaction with EUROPRACTICE was always helpful and constructive. Without them we would not have got our design ready for fabrication. This service seems to be unique in Europe and allows small players to benefit from global state-of-the-art fabrication facilities.

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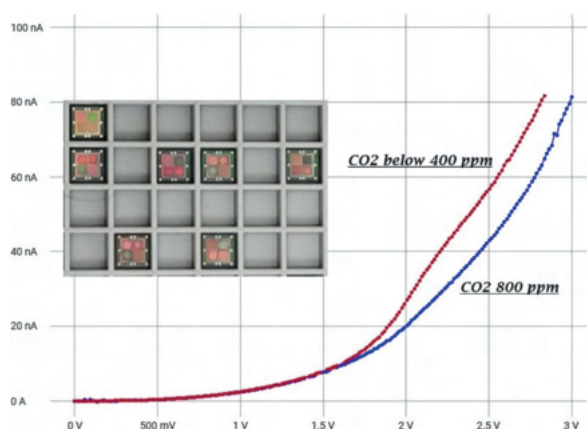[3] Electronic device for detection of viruses, bacteria, and pathogens, US 2017/0115252 A1, 2017 Apr 27.

Fig.3: Response of our CMOS sensor to CO_2 at room temperature. The concentrations were measured by a calibrated CO_2 sensor. The difference after 1.8 volts is clear and the change in current with concentrations is linear from 400 to 900 ppm after which it saturates. The dies obtained from EUROPRACTICE are also shown.

An ultra-low power PPG sensor based on Dynamic Photodiode (DPD)
ActLight SA, Lausanne, Switzerland

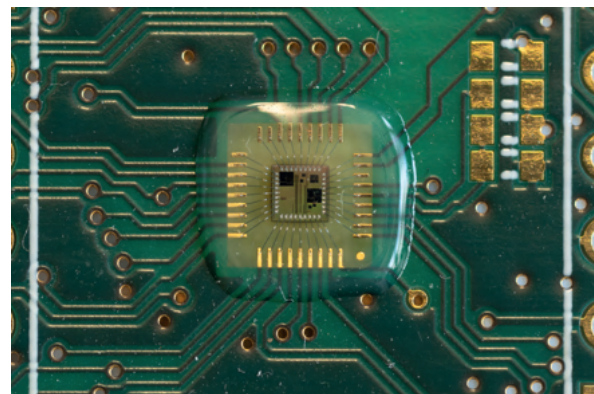|	
Contacts:	Evgenia Voulgari, Lucas Perrin
E-mails:	voulgari@act-light.com, perrin@act-light.com
Technology:	UMC L180 MM/RF
Die Size:	1.525mm x 1.525mm
Application Area:	Medical / Health

Fig.1: FRAISE ASIC.

Introduction

We developed this device to address the rapidly growing demand for small Vital Signs Monitoring sensors for wearable devices, focusing on the essential factors of very compact size and ultra-low power consumption. Our goal is to meet the market's need for efficient PPG sensors in smaller wearable devices such as smart rings and hearables, enhancing user experience and convenience.

Description

We have designed an ASIC named FRAISE based on our DPD (Dynamic photodiode) sensor that can be used for heart rate monitoring in wearables. The device offers low power consumption that leads to higher battery life. It can be miniaturized due to the small size of the sensor and the circuitry, and it can be manufactured in a standard process like UMC 180nm.

The DPD device does not operate as a standard photodiode where the current has to be amplified and measured. It works in dynamic mode, so first, the device is reversed biased, and then it is switched to forward mode. The device triggers due to incident light, and a strong forward current appears after some time. This delay, the triggering time is detected[1].
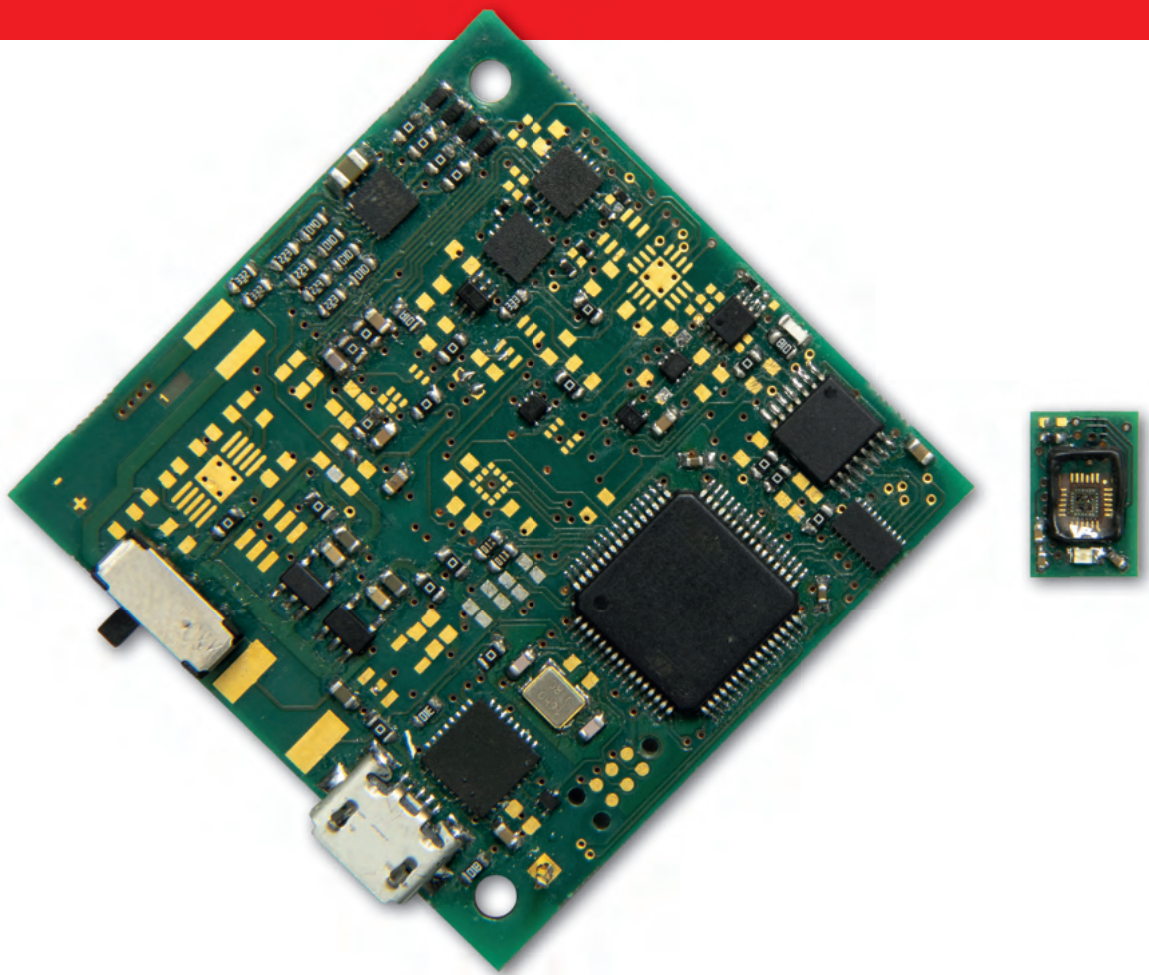
Fig.2: Typical demonstrator for PPG applications.

The front-end architecture is not based on an integrator that amplifies the generated current but it rather detects the triggering time directly in the digital domain. A custom tri-state buffer connected to the anode of the DPD followed by a PMOS transistor can detect the triggering of the sensor. This design leads to easier implementation of the circuit, smaller size, less noise and lower power consumption. The front-end requires a control signal that puts the DPDs either in reverse or in forward state, two biasing currents that supply the first and the second stage and the voltages that the anode, cathode and gate are biased. Eight different channels connected to different DPDs were designed for testing purposes, but each time, only one sensor and front-end were active. The others were in reverse biasing mode.

The DPD sensor is shot noise limited and has high Signal to Noise Ratio (SNR). The measuring system includes the DPD sensor with the front-end, the biasing circuits, the LED driver and a microcontroller. A TDC is measuring the triggering time that is inversely proportional to the light intensity. A graphical user interface (GUI) is used to control the circuit and visualize the data.

Results

The chip is working and providing the expected results. The actual focus is on optimizing the sensor for different target applications in healthcare/vital signs monitoring and wellbeing or fitness. The same technology and front-end can be also used in other high sensitivity optical sensing applications. Using mini@asic we were able to test different sensor geometries giving optimized performance for each application.

Why EUROPRACTICE?

EUROPRACTICE mini@asic runs allow us to easily test our technology on different foundries. This flexibility and wide offer of foundries is a key element in our test process, and the communication and support from imec have always been excellent.

References

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AnaSPAD: A camera with analog histogramming for photon counting
Universitat de Barcelona, Barcelona, Spain

Contacts:	Sergio Moreno, Victor Moro, Oscar Alonso, Angel Diéguez
E-mails:	sergiomoreno@ub.edu, vmoro@ub.edu, oalonso@ub.edu, angel.dieguez@ub.edu
Technology:	X-FAB XH018
Die Size:	4mm x 2.5mm
Design Tools:	Cadence
Application Area:	Medical / Health

Fig.1: Picture of the ASIC package "AnaSPAD1" with wirebonding.

Introduction

Single-photon avalanche diode (SPAD) image sensors have advanced to incorporate per-pixel functionalities suitable for a wide range of time-resolved applications. The predominant integrated per-pixel functionalities for temporal resolution applications include time-correlated single photon counting (TCSPC)[1], which typically relies on the accuracy of a time-to-digital converter (TDC), and single photon counting (SPC)[2]. These techniques can be implemented using analog or digital circuits. The complex digital processing required for TCSPC pixels results in a large pixel area with a small proportion dedicated to SPAD, leading to a decrease in sensitivity. On the other hand, data rates tend to be low because most of the data processing takes place off-chip. An alternative approach is on-chip histogram generation, which improves data throughput. Analog processing overcomes the area limitation of digital implementations and offers a compact solution by counting photons in the charge domain.

Description

The ASIC described in this article integrates the analog generation of a histogram for photon arrival times using X-FAB 180nm technology. Thus, the chip consists of three main blocks. A 12x16 SPAD camera of 150x150µm^2 pixels with random access, and serial output is the sensing part. Each pixel incorporates an analog histogramming circuit. Then a TDC based on Vernier architecture allows the classification of the photons in the in-pixel histogram. A single slope ADC digitalizes the analog value stored in the hitogramming circuit of each pixel. The pixel design of the camera incorporates techniques to reduce the leakage (from ~pA to ~fA) to achieve a histogram of 16 bins and an accuracy of up to 8 bits.
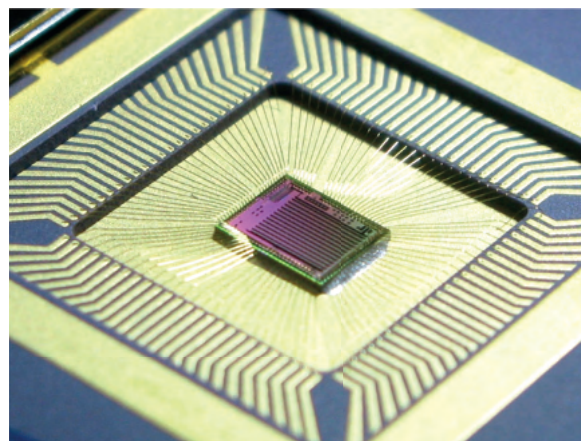
In addition, additional SPAD structures are designed for testing purposes.

Results

The chip was received in September, and it is still under test.

Why EUROPRACTICE?

EUROPRACTICE provides affordable access to various foundries and design tools, offering prices that suit researchers and institutions. In our case, EUROPRACTICE allows us to participate in MPW runs, allowing us to integrate and test both our designs and test structures needed for our research projects.

Acknowledgements

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Servo Drive Controller ASIC
Rosenheim Technical University of Applied Sciences, Rosenheim, Germany

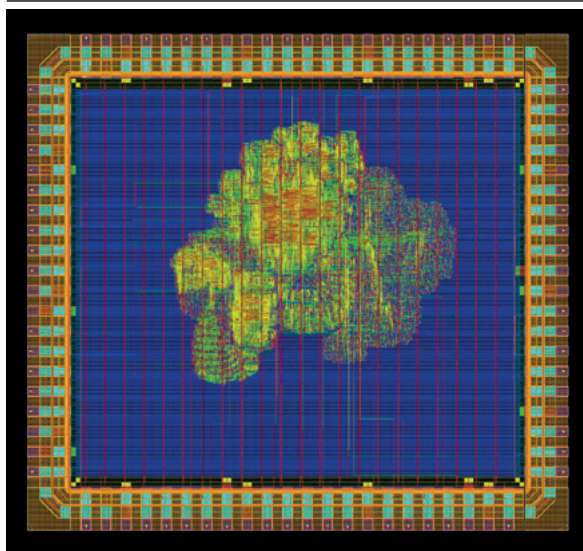|	
Contacts:	Markus Märkl, Stefan Höltl, Martin Versen
E-mail:	martin.versen@th-rosenheim.de
Technology:	X-FAB XH018
Die Size:	3.230mm x 2.965mm
Design Tools:	Cadence Virtuoso, Genus, Innovus
Application Area:	Manufacturing / Industry 4.0

Fig.1: Layout view of the servo drive controller.

Introduction

Position-controlled servo drives are widely used in automation systems. Usually, a cascaded control structure with a position, speed, and a current controller as the innermost control loop are used. Pulse-width-modulation (PWM) frequencies above 100kHz, in combination with fast control algorithms, are required for high-dynamic and low-latency motor control systems. The goal was to use model-based development entirely to design the ASIC for this application.

Description

A controller usually consists of proportional, integral and differential (PID) elements, the motor control ASIC is a configurable PID controller. The configuration is achieved by a serial peripheral interface (SPI). The servo motor controller acts as an SPI slave. Digital inputs connect to three delta-sigma modulators, which sample at an input frequency of 16MHz. One analog input receives a current input signal, while the other two interface to the A/B signal of a rotary or a linear encoder. Three sinc3 decimation filters are implemented with variable filter lengths between 16 and 64 to reduce the noise of the serial 1-bit input data streams. For the motor control, the output signal switches to a full-bridge assembly with an adjustable resolution of up to 16bit with a device frequency of 100MHz. The project includes a digital output interface for two 16bit digital-analog converters (DAC) so that we can visualize control loop variables with an oscilloscope on-line.
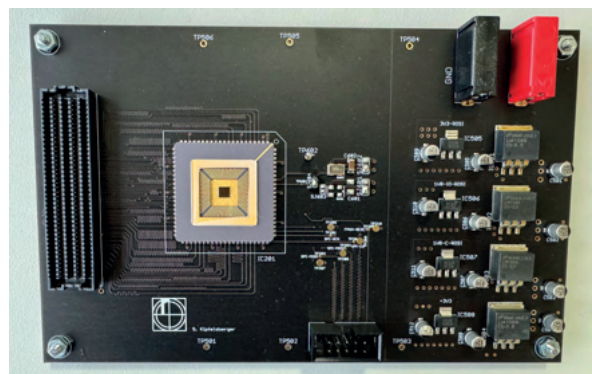

Fig.2: Photograph image of the servo drive controller on a motor control board.

Results

The servo drive control ASIC is 100% successfully tested. We can use the individual control loops for PWM-frequencies up to 200kHz. In combination with a position measuring device with a signal period of 4µm, a position stability of a linear voice-coil motor of +/-1.6 nanometer is reached in position-controlled stand-still mode. This value was previously also achieved with an FPGA implementation and delta-sigma analog-to-digital converters (ADC). With successive approximation ADC, an even higher position stability can be reached. The ASIC will be used in lab practices for mixed signal systems in the university's master's program.

Why EUROPRACTICE?

The Rosenheim Technical University of Applied Sciences has licensed Cadence Tools through EUROPRACTICE for several years. EUROPRACTICE's technical support for chip submission and chip packaging has benefitted us. EUROPRACTICE has given us affordable access to a multi-project wafer fabrication run.

Fig.1: Microphotograph of the fabricated chip.

A Sensor Interface IC for Fluxgate Magnetometers

Institute of Electrical Measurement and Sensor Systems, Graz University of Technology – Space Research Institute, Austrian Academy of Sciences, Graz, Austria

Contacts:	Maximilian Scherzer, Mario Auer, Aris Valavanoglou, Werner Magnes
E-mail:	maximilian.scherzer@tugraz.at
Technology:	X-FAB XH018
Die Size:	3.04mm x 1.52mm
Design Tools:	Cadence
Application Area:	(Aero)Space

Introduction

Fluxgate magnetometers are commonly used sensors for space missions, particularly for planetary exploration. Numerous successful space missions have probed various planetary and interplanetary magnetic features, confirming this preference. However, achieving accurate measurements requires a dedicated electronic circuit. This involves processing the signal from the sensor and converting it to digital data using an analog-to-digital converter. To enhance accuracy and stability, the sensor's ambient magnetic field is cancelled out by a feedback loop. However, existing space-qualified circuits often rely on a mix of discrete components, which limits their performance. Space electronics must be lightweight, compact, power efficient and able to withstand extreme conditions such as temperature variations and radiation. The use of integrated circuits offers the best solution to meet these challenging requirements.

Description

The designed chip features a digitally controlled, fully differential, low-noise current source. It has been designed for use in the feedback path of a fluxgate magnetometer, although the concept is applicable wherever a low noise and accurate current are required. The digitally controlled current source consists of a novel current amplifier that is driven by a current-steering digital-to-analog converter as presented in [1]. In addition, the chip contains an analog lock-in amplifier that can efficiently read out the magnetic field information by applying the principle of N-path filtering as reported in[2].

Results

Several chip samples were characterized using an experimental setup including an Audio Precision APx555 analyzer.
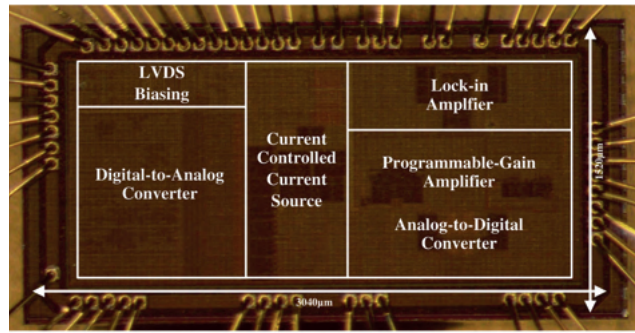
The implemented current source has two output ranges ("high range" and "low range"). The maximum measured signal-to-noise ratio for a bandwidth of 512Hz is 105.2dB for the "high range" and 103.8dB for the "low range". However, the performance of the current source is limited by the total harmonic distortion of -94.8dB for the "high range" and -90dB for the "low range". The measured noise floor at 1Hz is less than 4.5nA/Hz for the high range and less than 3nA/Hz for the low range. Depending on the sensor used, a theoretical noise level of 11.1pT/√Hz at 1 Hz can be achieved. In summary, the advantage of the proposed digitally controlled current source is that it consumes a minimal power of 46mW while remaining linear at high field amplitudes. Further, the operating principle of the lock-in amplifier has been validated using an experimental setup. In contrast to existing solutions, the center frequency is tunable from 10 to 100kHz and reaches a bandwidth of 0.4 to 4kHz while maintaining a low power consumption of 1.8mW at 1.8V.

Why EUROPRACTICE?

The Graz University of Technology – Institute of Electrical Measurement and Sensor Systems – has worked with EUROPRACTICE for several years. EUROPRACTICE Services provide access to design support and process design kits. Besides, EUROPRCATICE offers excellent technical support for DRC verification and GDS submission. Finally, EUROPRACTICE provides access to different technologies at affordable prices.

Acknowledgements

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SKY-IC-RHLCL-A1: Radiation Hardened Latch-Up Current Limiter ASIC

SkyLabs d.o.o., Maribor, Slovenia

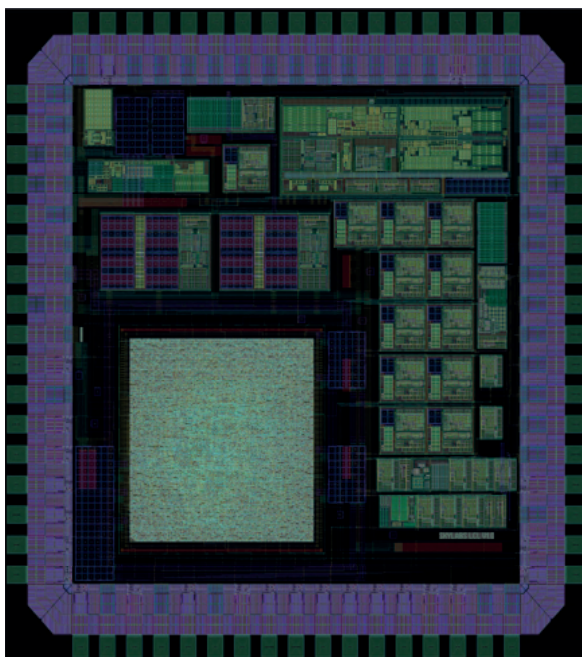|	
Contacts:	Bojan Kotnik, Matic Erker
E-mails:	bojan.kotnik@skylabs.si, matic.erker@skylabs.si
Technology:	X-FAB XT018
Die Size:	2.146mm x 2.146mm
Design Tools:	Cadence Virtuoso, Spectre, Genus, Innovus
Application Area:	(Aero)Space

Fig.1: Layout of SKY-IC-RHLCL-A1 ASIC.

Introduction

SKY-IC-RHLCL-A1 is especially designed to protect and supervise modern COTS FPGAs used in on-board data handling and in other satellite systems.

Several voltage rails are typically required to power up a modern FPGA typically ranging from 0.9V up to 3.3V. Furthermore, FPGA manufacturer also precisely defines the timings and power-on sequencing of these rails. The power management of FPGAs is thus a complex and delicate task. This is valid especially in Space applications, where adequate latch-up protection due to adverse radiation effects also needs to be considered.

Besides being able to protect the FPGA in case of SEL, SKY-IC-RHLCL-A1 embeds also one important feature for mission critical applications: An integrated SEFI watchdog functionality.
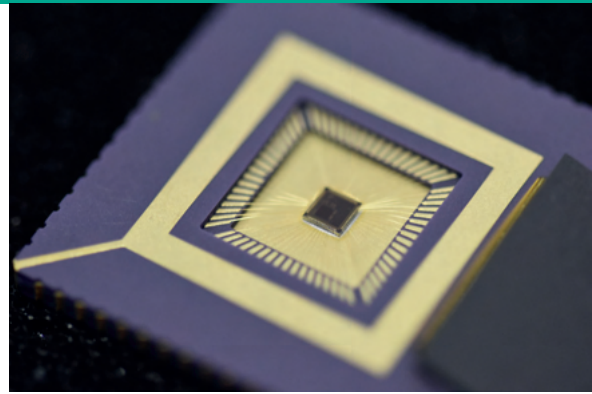

Fig.2: Photograph of the packaged die (CLCC68 package).

This watchdog requires a periodical clearing from the protected component. In case of watchdog expiration, SKY-IC-RHLCL-A1 will either power-off, or power-cycle (depending on configuration) the protected component.

From the electrical current limitation perspective, SKY-IC-RHLCL-A1 also provides highly flexible configuration. Two different current limitation periods can be independently configured (the current limits as well as the corresponding timings): the in-rush period, and nominal operational period. Last but not least, SKY-IC-RHLCL-A1 embeds also SPI interface where the telemetry readouts can be made. Furthermore, the power-on default parameters, such as overvoltage limit, current limits, and all timing parameters are pre-defined, but with variety of options. RHLCL2022A1 embeds the flexibility to change these defaults also via SPI interface.

Description

SKY-IC-RHLCL-A1 ASIC die consists of the following main blocks:

- Analog Subsystem. This Analog IP module contains the Current Sense Amplifier, Overcurrent Detection Circuit, Power-on Default parameters capture block, RC-oscillator based clock generator, and Power-On Reset IP block.
- High Power and Power Supply Subsystem. This Analog IP block contains external power PMOS/NMOS regulation including the respective configurable compensations, the driver for external discharge BJT, a linear dropout regulator to generate internal supply voltage, a bandgap voltage reference (for ADCs, DACs), and an internal temperature sensor with thermal protection.
- Telemetry Subsystem. This subsystem consists of Analog IP frontends of Delta-Sigma Analog-to-Digital, and Sigma-Delta Digital-to-Analog converters. SKY-IC-RHLCL-A1 contains 12 ADCs: 8 of them are utilised to capture the values from external components, defining the power-up default parameters (over- and under voltage thresholds, in-rush and operational current limits, inrush- and trip off time durations, autostart delay, and chain-out delay). Four ADCs are dedicated for telemetry purposes (current monitor, input- and output voltage measurement, and die-temperature measurement). The two DACs define the current limit (in-rush current limit
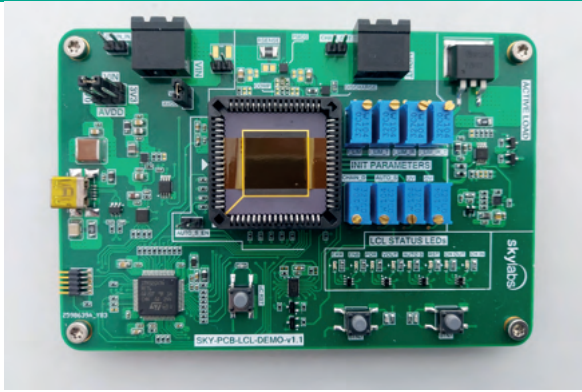
Fig.3: Evaluation and Demo Board with SKY-IC-RHLCL-A1 ASIC.

during in-rush period, or operational current limit otherwise), and the input overvoltage threshold, respectively. Due to the inherent slow-speed nature of Delta-Sigma ADC, the overcurrent detection is done directly in Overcurrent Detection Circuit Analog IP using a fast comparator.

Digital Core IP implements the main Finite State Machine (FSM), register file, SPI communication interface, timers, internal signal control logic, and chain-in/chain-out signal control.

The development of analog IP modules (from schematics to layout, including all pre- and post-layout simulations, corner analysis, and Monte Carlo simulations) as well as the chip's top-level floorplanning and pad-ring integration have been done in Cadence Virtuoso. Due to the analog part of the chip being comparatively larger than the digital core, the Analog-on-Top (AoT) paradigm was followed.

Results

The first 50 prototypes have been manufactured and successfully brought up. Detailed electrical characterization of the devices is showing consistent results when compared to pre-silicon simulations. Part-to-part deviations are nominal and within expected margins. In the beginning of 2024, we will proceed also with radiation characterizations in order to evaluate Total Ionizing Dose (TID) robustness and SEE immunity of the ASIC.

Why EUROPRACTICE?

EUROPRACTICE provides affordable access to the design tools under the Proof-of-Concept (PoC) licensing scheme and offers fabrication and packaging of our very first ASIC prototype in MPW shuttle.

Acknowledgements

References

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Key Cells for In-Field Optimizable and Adaptive Spiking Analog Front-Ends with Self-X Properties

RPTU Kaiserslautern-Landau, KISE, Germany

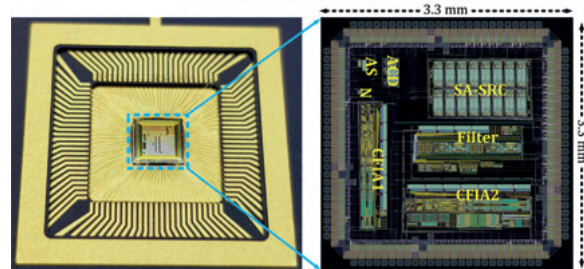|	
Contacts:	Senan Alraho, Qummar Zaman, Hamam Abd, Andreas König
E-mail:	koenig@eit.uni-kl.de
Technology:	X-FAB XH035
Die Size:	3.3mm x 3.3mm
Design Tools:	Cadence
Application Area:	Manufacturing / Industry 4.0

Fig.3: (A) Manufactured chip (B) Chip layout.

Introduction

Sensor and sensory systems gain in importance in technical systems, in particular, in conjunction with machine-learning for smart system realization [5]. Analog-front-ends (AFE) are needed in a rich variety and agility to serve the quite heterogeneous sensor field. AFE are needed in discrete shape for off-the-shelf solutions as well as cells for large scale highly integrated solutions. The forefront technology nodes impose increasing challenges on analog design [4]. For instance, keeping up amplitude domain representation and processing of information becomes constantly harder. Both in-field optimizable circuits and evidence from the peripheral nervous system and biological sensing offer promising approaches [6][7]. The fabricated device follows up to previous comprehensive AFE chips manufactured via EUROPRACTICE (Universal-Sensor-Interface with self-X properties, USIX). The recent device embodies new concepts for amplitude (Fig. 1) and spike domain information representation with a reduced complexity for proof-of-principle (Fig. 2).

Description

Machine-Learning/AI techniques and bio-inspiration are employed for both optimizing the design and inspiring the designs themselves. A particular focus is on so-called Self-X- or Self-*-systems, which translate steps of the design time
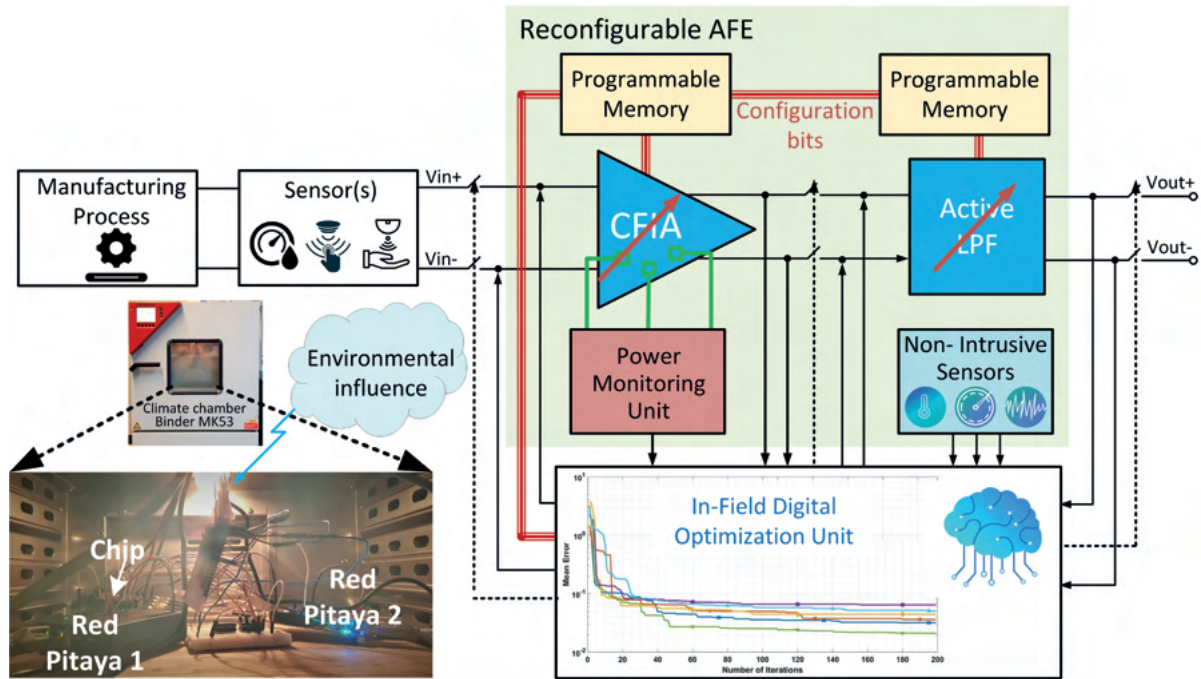
Fig.1: Lean In-Field Optimizable Analog Front-End with Self-X Properties.

optimization into the run time by giving adaption and/or reconfiguration resources and harvesting more reliable, accurate, and robust solution better meeting metrology constraints. The device designed and fabricated hosts essential building blocks of reconfigurable in-field optimizable amplitude domain circuits, such as reconfigurable indirect current-feedback in-amp (CFIA), CFIA with programmable AAF, and non-obtrusive sensors for AFEX as well as spiking neuron cells and adaptive coincidence detectors for SAFEX in X-FAB XH035 CMOS technology (Fig. 3). Extrinsic optimization and/or adaptation have been employed in the design phase [1]. The chip features 62,921 transistors, a total area of 10.89mm^2 (74% analog, 26% digital), and 66 bytes of the configuration memory. The prepared demonstrator was tailored to allow intrinsic optimization and/or adaptation for the developed technology agnostic concepts and chip instances.

Results

For testing of both AFEX and SAFEX cells, two demonstrators [2,3] were created based on Red Pitaya systems and DUT PCBs. For AFEX [2], bit patterns from extrinsic optimization were employed for investigations. Intrinsic or in-field optimization employing an efficient PSO variant was successfully conducted
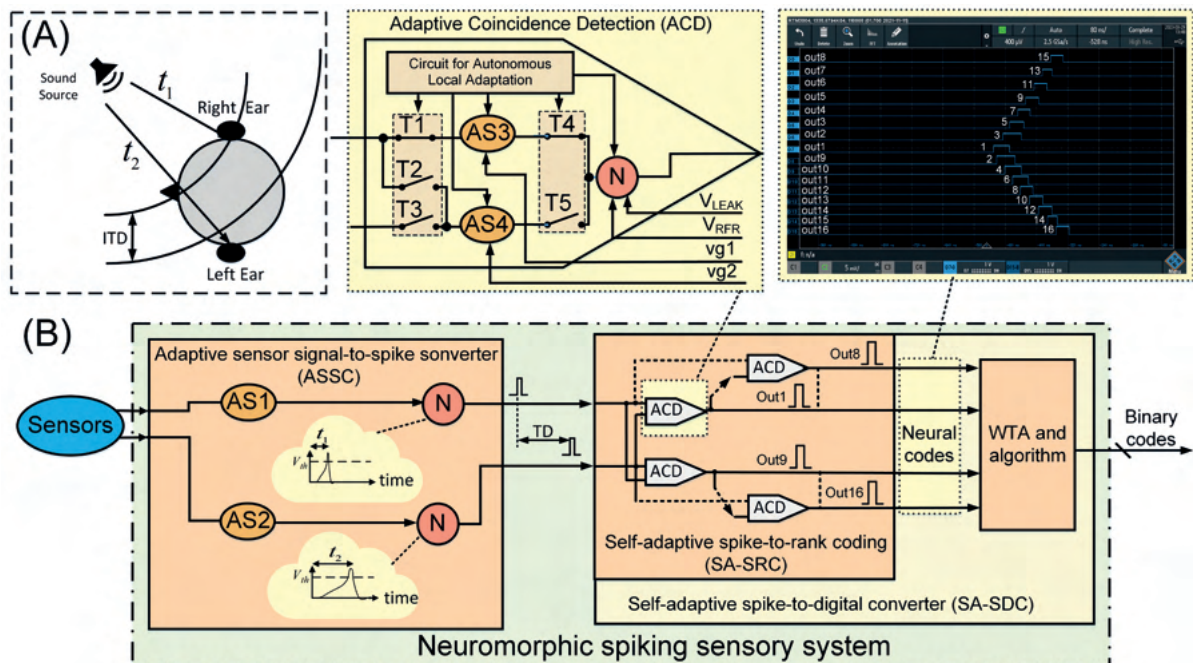

Fig.2: (A) Acoustic localization model (B) Proposed neuromorphic spiking sensory system.

for the CFIA based on THD and non-intrusive sensor concepts, both under temperature variation in a Binder climate chamber and for 15 different chips from the manufactured batch [2]. Programmable AAF experiments are not yet completed, but all cells display the needed functionality. For SAFEX [3], this could also be confirmed. For the key cell, the self-adaptive spike-to-rank coding (SA-SRC) with its first level of adaptivity and 4-bit resolution the expected conversion behavior and the quality increase due to adaptation, also after perturbations, could be demonstrated, e.g. INL/DNL values before and after adaptation were 4.4/1.53 LSB, and 0.46/0.4 LSB, respectively. LIF-neurons and synapse circuits, which serve for sensor-to-spike conversion purpose SAFEX in ongoing work, performed also fine. The SAFEX concepts are expected to really bear fruits moving them from 350nm to advanced FinFET technology of 12nm or smaller.

Why EUROPRACTICE?

EUROPRACTICE provides both the access to the required design tools and PDKs of established to high-end technologies. The well-guided translation to a physical design at affordable cost allows to do explorative research without the need for acquiring substantial funding.

Acknowledgements

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A Photonic Extreme Learning Machine

Nanoscience Laboratory, Department of Physics, University of Trento, Trento, Italy

Contacts: Stefano Biasi, Riccardo Franchi and Lorenzo Pavesi
E-mail: lorenzo.pavesi@unitn.it
Technology: AMF Si-Photonics
Die Size: 7.85mm x 3mm
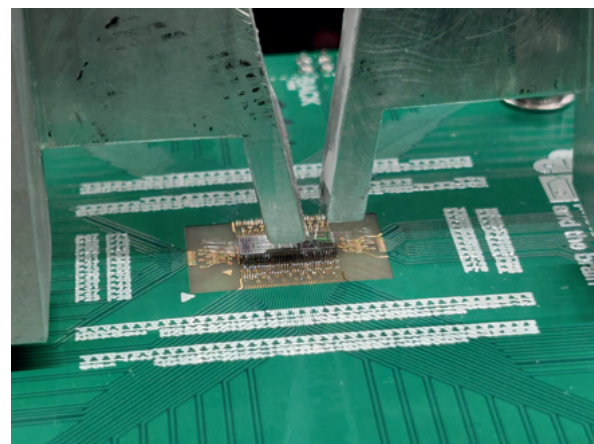**Application Area:** AI

Fig.1: The chip wire bonded and mounted on the PCB under the testing setup. The two metal holders for the input/output optical fibers are also observed.

Introduction

Photonics has demonstrated state-of-the-art performance in challenging computational tasks. Indeed, photonic integrated circuits (PICs) could meet the demand for scalability by mitigating power consumption. One widely used machine learning algorithm is the feed-forward neural network (FFNN). FFNNs have been integrated in silicon photonics and have shown excellent performances compared to their electronic counterpart [1]. However, training these networks is power-hungry and time-consuming because of the many parameters to be optimized. Promising alternatives are neural networks that do not require full control of all the node interconnections, such as the Extreme Learning Machines (ELM) [2]. The ELM is a FFNN consisting of a single hidden layer where training occurs only at the readout stage. The design we present aims at a PIC which implements the computational paradigm of an ELM to get better performances than its electronic counterpart.
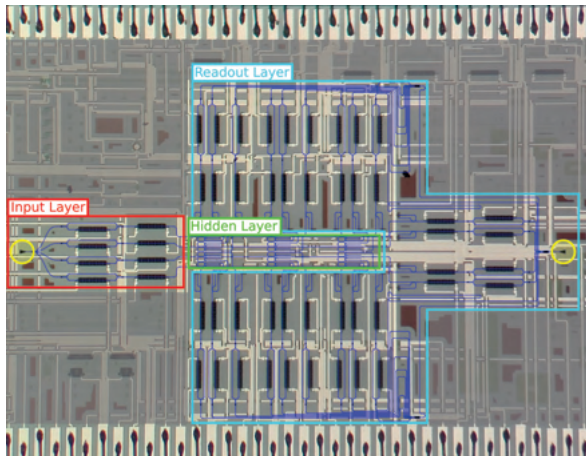
Fig.2: Optical image of the part of the chip that realizes the photonic ELM neural network. The blue lines indicate the optical paths, i.e. the waveguides and microresonators. The input and output gratings are highlighted by the yellow circles on the very left and very right, respectively. The input, hidden and readout layers, are highlighted by red, green and light blue contours, respectively.

Description

The PIC wire-bonded on a board under the testing setup is shown in Figure 1. The photonic ELM is shown in Figure 2. It contains an input layer where the information is encoded, a hidden layer formed by an array of 18 microresonators, and a final readout layer consisting of a linear classifier (LC). Thus, all the steps, from data encoding to network training, take place in the PIC. In the input layer, a single grating is used to insert the CW optical signal at 1550 nm. Here, the optical signal is routed to four waveguides along which a series of a Mach–Zehnder interferometer (MZI) and of a phase shifter (PS), both actuated by microheaters, is used to encode the input data on the optical signal. Then, the four waveguides are coupled to a 3x3 array of pairs of coupled microresonators in the hidden layer. Each microresonator has a tap to collect 5 ‰ of the circulating intensity. The 18 taps and the four waveguides in the array rows feed the LC stage. This consists of a cascade of 22 MZIs in series with 22 PSs that are recombined in a single output grating coupler. During the training, the real and imaginary parts of the weights are applied by current injection in the thermal heaters of each MZIs and PSs. Moreover, to facilitate the training, each of the 22 LC inputs has a tap connected to an integrated fast photodetector. Nonlinearity in the photonic ELM is provided by the microrings and the reading photodetector.

Results

A first proof-of-concept demonstration of the microresonator-based ELM is reported in [3]. Here, the PIC has integrated only the encoding and the microring array. The scattered light from the hidden layer is recorded by a camera. The analysis of the camera images allows to perform the LC offline. Common benchmarks are solved with high performances though with a low operational speed. The novel fully integrated PIC design is still under test while we anticipate better performances and operational speed.

Why EUROPRACTICE?

AMF Si-Photonics through EUROPRACTICE allows us to manufacture our chip due to i) the variety of active and passive component PDKs, ii) the correspondence between nominal and manufactured values, and iii) their strict adherence to the six-month delivery date, which makes our research more streamlined.

Acknowledgements

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Photonic Integrated Millimiter Wave Band RF Synthesizer
Scuola Superiore Sant'Anna, Pisa, Italy

Contacts:	Claudio Porzi, Antonio Malacarne, Antonella Bogoni
E-mail:	claudio.porzi@santannapisa.it
Technology:	imec Si-Photonics iSiPP50G
Die Size:	5mm x 5mm
Design Tools:	Luceda IPKISS
Application Area:	Datacom / Telecom

Introduction

Spectrally pure RF carriers in the millimeter wave- and sub-THz bands are of great interest for modern wireless communications and sensing systems. Photonics-based generation of RF carriers offers the advantages of wide tunability, low phase noise characteristics, and low-loss signal distribution over optical fiber links. Photonic integration brings the additional advantages of compactness, stability, and reduced fabrication costs. A suitable electro-optic packaging approach is also required for practical applications.

Description

The circuit operates as a frequency multiplier of an input reference microwave local oscillator (LO) signal. The LO is applied to the RF input port of the circuit, where an on-chip optical frequency comb (OFC) source generates a comb of optical tones spaced by the LO frequency around a laser carrier which also enters the circuit from its optical input port.

A tunable photonic integrated bandpass filter is then used to select one tone from the OFC spectrum, while strongly suppressing all the other spectral components. The selected comb tone is then recombined with a replica of the original laser carrier. Two optical tones spaced in frequency by an integer multiple of the LO frequency are then retrieved at the optical output port of the circuit. A high-speed photodiode (PD) after a distribution fiber link then generates the millimeter-wave/sub-THz RF carrier.

Results

By applying a 20 GHz LO reference signal at the input port of the on-chip OFC source and selecting the 5th-order comb harmonic through the photonic integrated filter, a 100 GHz RF carrier is generated using an external PD. The phase noise performance of the generated W-band clock is evaluated through a signal source analyzer. The results indicate an operation in line with that of an ideal frequency multiplier, with limited excess phase noise introduced by the circuit resulting in a measured time jitter which is less than 2 fs than that of the reference LO. The improved phase noise performance with respect to other reported photonic-integrated approaches based on free-carrier laser sources is promising for increasing the channel capacity and the spatial resolution for communication/sensing operations in next-generation wireless systems.
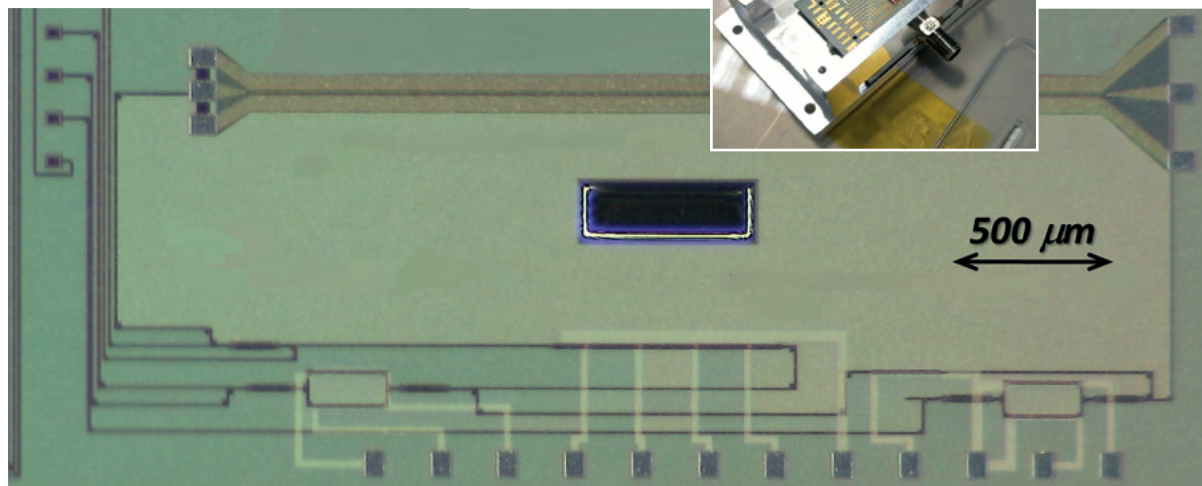

Fig.1: Micrograph of fabricated photonic integrated circuit and picture of fully electro-optic packaged device.
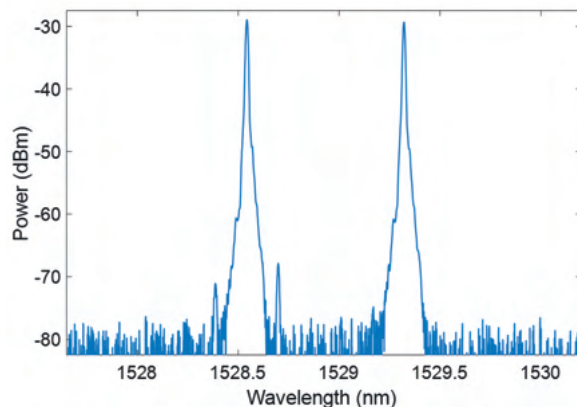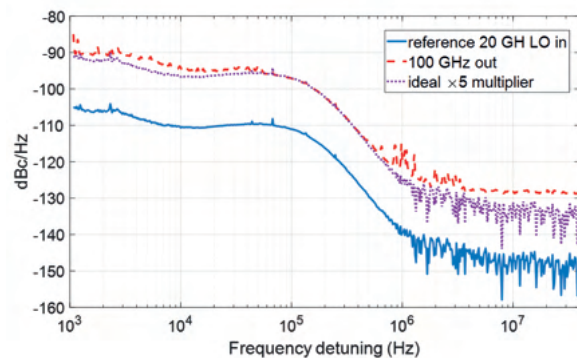
Fig.3: Single-sideband phase noise power spectral density of the generated 100 GHz carrier after photodetection (dashed line) and of the LO input signal (solid line). The case of ideal LO frequency multiplication is also shown (dotted line).

Why EUROPRACTICE?

Access to reliable fabrication process for the development of prototype devices based on photonic integrated circuit technologies.

Acknowledgements

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PIC-based temperature sensor enabling smart composite manufacturing

Institute of Communication and Computer Systems, Athens, Greece

Contacts: Giannis Poulopoulos, Georgios Syriopoulos, Evrydiki Kyriazi, Harry Zervos, Hercules Avramopoulos

E-mails: jpoul@mail.ntua.gr, georgesyriopoulos@mail.ntua.gr, evkyriazi@mail.ntua.gr, hzervos@mail.ntua.gr, hav@mail.ntua.gr

Technology: imec Si-Photonics Passives+
Die Size: 5mm x 5mm
Design Tools: Luceda IPKISS
Application Area: Manufacturing / Industry 4.0

PIC sensor embedded in composite tool
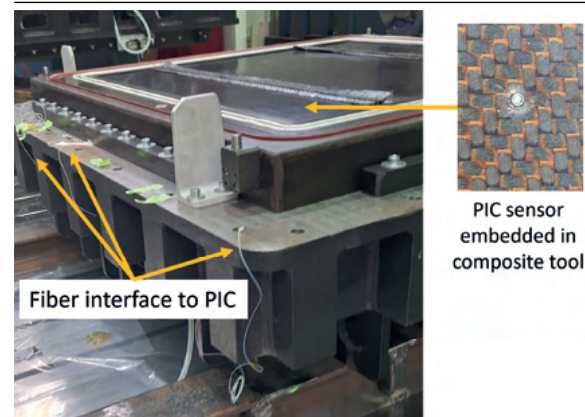
Fiber interface to PIC

Fig.1: PIC sensors embedded in composite tool.

Introduction

In the aerospace industry, composite materials are gaining ground all the time, consisting of more than 50% of the aircrafts now. However, these composite parts are required to be of high quality and have very strict rules for process monitoring and quality control. Photonic sensors are key in this process since Carbon Fiber based composites have issues with using electrical sensors for measuring at the composite surface. We have shown a Photonic Integrated based sensor that is measuring temperature at the composite surface up to 180℃ and 3 bar, while it is embedded in a composite tool (bypassing the need of power-hungry autoclaves). Our design is compatible with a multi-sensor configuration, allowing the measurement of Refractive Index (cure state) and pressure, two values that are still elusive in the composite manufacturing industry. Using all three measurements in many different areas of the composite part enables advanced optimisation techniques based on

smart algorithms with estimated reduction in the processing time in the order of 30% (Figure 1).

Description

The multi-sensor designed targets to measure temperature (T), Refractive Index (RI), and Pressure (P). It is composed of 3, in series connected Bragg grating elements, shown in Figure 2, centered at different wavelengths in C-band region, touching the manufactured composite part. Optimised Bragg grating elements were designed, employing phase-shift, to increase the accuracy of the measurements.

A standard grating coupler is fabricated at the center of the chip, to allow high efficiency fiber-to-chip backside optical interfacing. The 1st Bragg grating is fabricated in a circular geometry, enabling after post-processing the formation of a membrane, implementing a strain sensor by measuring equal deformation of the Bragg period across its whole length. We have good results from the circular Bragg structures (varying with temperature), showcasing the possibilities of using the MPW with non-standard elements.

A 2nd Bragg grating element in series is centered at a different wavelength. This sensor was post-processed to remove the on-top protective oxide, exposing the Bragg element to the under-test resin material. This allows to measure the resin's RI while the fundamental mode evanescent field propagates within the resin material. It is important to note that this process was not available in the MPW we participated in, however, this is part of the available processes now and of great interest to sensing applications.

The 3rd Bragg sensor targets to measure the temperature change, which affects the Effective RI of the silicon waveguide, resulting in a resonance wavelength red-shift. This 3rd sensor will also act as a reference measurement for the red-shift that the RI and P sensor will experience due to the temperature variations.

Results

After the fabrication of the chips, a detailed evaluation was carried out in the Photonics Communications Research Laboratory (PCRL/ICCS) regarding the temperature response in good agreement with the simulation. Up to 180°C the sensitivity was 81 pm/°C.

After dicing, the sensors were assembled by ARGOTECH in a rod packaging module, employing a ball-lens interface for back-side fiber-to-chip interconnection developed and tested by imec [1]. The packaged sensors were integrated in composite tools.
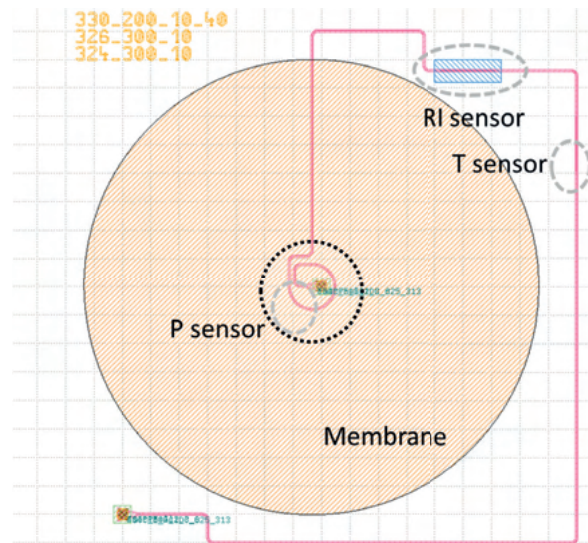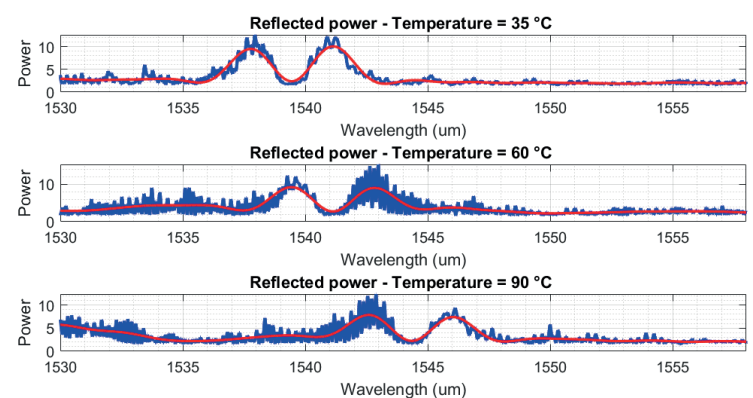

Fig.2: Mask layout of multi-sensor.

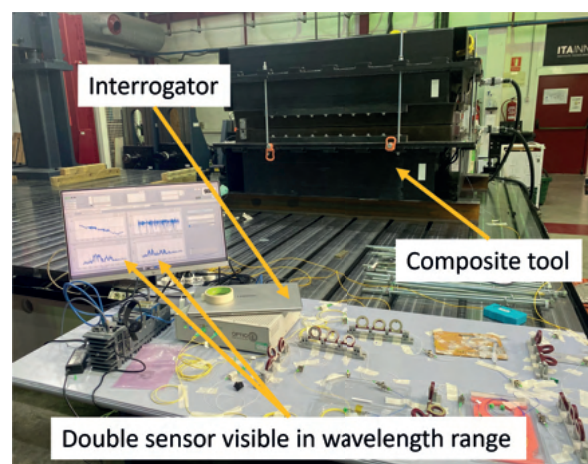Fig.3: Reflection spectrum throughout fabrication process.

Fig.4: Validation of the sensing system.

The composite tools were used to manufacture several composite parts under relevant industrial conditions both in the UK and Spain. Monitoring the sensors throughout the entire fabrication process [2], including preparation of tool, preheating, injection, curing and cooling cycles (Figure 3), validated the operation and stability of the sensors as temperature sensors (Figure 4). RI and P sensor post-processing is ongoing.

Why EUROPRACTICE?

EUROPRACTICE provides access to several integration technologies, enabling designers to select the one that is best suited for their needs. For our case, we had access to imec's Passives+ MPW run, where we fabricated our designed multisensor on imec's thin-SOI integration platform.

Utilising the PDK at the time, we managed to fabricate working temperature sensors and validated them in an industrial environment. In addition to the PDK, we managed to include innovative design in our circuits that were also successfully validated (i.e. Bragg gratings in circular topology).

Finally, within the premises of a European project close to the industrial application, utilising an MPW run showcased that fabricating PIC-based sensors is scalable, significantly reducing the overall cost utilising commercially available fabrication services.

Acknowledgements

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Multi-MHz Auto-Resonant Power Oscillator in a 650 V GaN-on-SOI Technology for Compact Wireless Power Transfer Systems

Institute of Robust Power Semiconductor Systems, University of Stuttgart, Stuttgart, Germany

Contacts:	Manuel Rueß, Dominik Koch, Ingmar Kallfass
E-mail:	manuel.ruess@ilh.uni-stuttgart.de
Technology:	imec GaN-IC 650V
Die Size:	2.5mm x 2.5mm
Design Tools:	Cadence Virtuoso
Application Area:	Energy
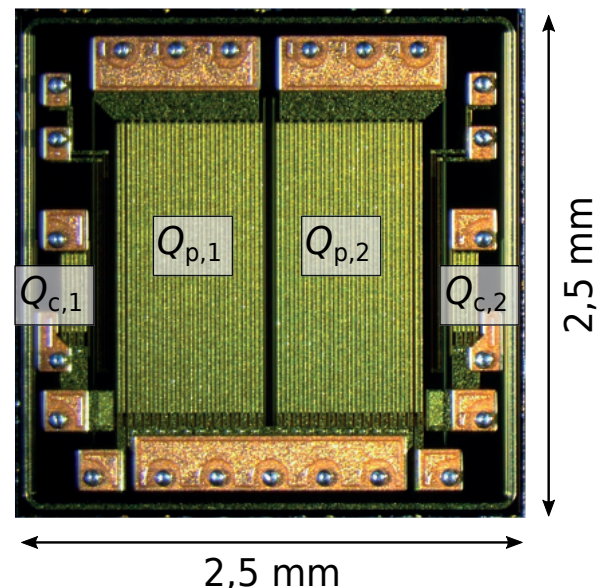
Fig.1: Design of the GaN-Royer IC, containing all active components.

Introduction

The design aims to optimize wireless power transfer (WPT) in the MHz frequency range. Compared to conventional transformer frequencies, between 20 kHz and 200 kHz, much higher frequencies in the MHz range allow the use of coils with much better properties. With the help of GaN and efficient power electronics, it is therefore possible to improve WPT systems in terms of efficiency, power density and costs.

Description

On a 2.5mm x 2.5mm area, the IC incorporates the switching cell of a Royer-Circuit [1]. Inverters and rectifiers for a WPT system can be designed with the help of this type of chip. The system is fully auto-resonant and does not require active

Fig.2: Output power and achieved efficiency of the WPT system at different resonant frequencies and load points.

circuits such as drivers. With the help of GaN technology, the resonant frequencies can be increased by a significant factor without increasing power losses.

Results

A WPT-System based on the auto-resonant 650 V GaN-on-SOI power oscillator was realized. Operation and performance of the system could be demonstrated at resonant frequencies of up to 3 MHz at input voltages reaching 60 V and output powers of ma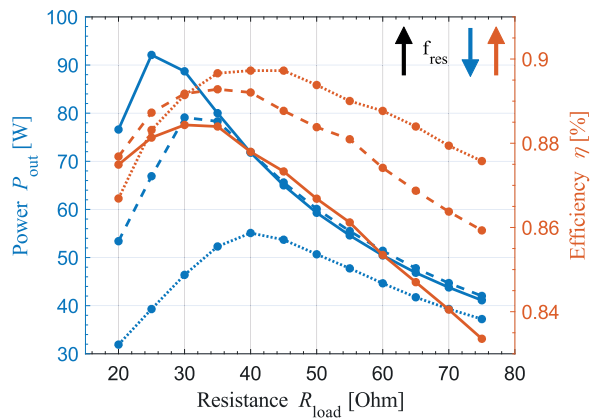x. 100 W. The combination of switching frequencies at 3 MHz and an efficient converter design allows for a very compact and cost-effective WPT-System, reaching efficiencies between DCin and DCout of up to 90 %. [2]

Why EUROPRACTICE?

EUROPRACTICE enables easy and uncomplicated access to various MPW runs. This enabled us to realize our design in the 650 V GaN-on-SOI technology provided by imec. During the design phase, we received very good support in answering questions and solving problems.

Acknowledgements

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MICAS: Advancing state of the art using EUROPRACTICE design tools and fabrication services

MICAS, Department of Electrical Engineering, KU Leuven, Belgium

Designers: MICAS research division at KU Leuven

Contacts: Prof. Wim Dehaene, prof. Georges Gielen, prof. Patrick Reynaert, prof. Michiel Steyaert, prof. Filip Tavernier, prof. Marian Verhelst; David Maes, Research Valorization Manager

E-mail: david.maes@kuleuven.be

At KU Leuven, the research on integrated circuit design has been ongoing for many decades, creating a large impact, both at the academic level and at the socio-economical level. MICAS, the chip research division of the Department of Electrical Engineering in Leuven, is a frequent customer of EUROPRACTICE, with several tape-outs each year in various technologies. EUROPRACTICE enables MICAS to characterize real devices and is therefore crucial to validate its research.

MICAS and its research approach

The research of MICAS spans a broad range, from conceptual blue-sky research, over applied research, up to partner-specific industrial research. In each phase of this pipeline, the research goes through every step in the design cycle: from system-level conceptualization and architecting, over integrated circuit design and implementation, to fabrication, packaging, and characterization. In this way, the initial idea spirals upward until it reaches its final goal: Creating academic and socio-economic impact. The academic impact is shown in scientific publications, while the socio-economic impact is obtained by transferring the research results through collaborations with industrial partners or through the creation of spin-offs.

The importance of real silicon in advanced technologies

Fabrication of the circuits is crucial for the success of MICAS, as real-life silicon is absolutely necessary to experimentally validate the research results. Without real chips, it is impossible to prove that the concepts, architectures, design and packaging approaches that are investigated are viable. The proof of the pudding is in the eating, but no eating without pudding. Without silicon validation, MICAS would not be able to convince potential industrial partners/customers. In short, valorization of the research results would be impossible. This implies that chip fabrication enables MICAS to stay relevant and attractive to the industry, to keep its capability to generate groundbreaking academic output, and to attract international talent.

The role of EUROPRACTICE in the research activities of MICAS

The continuation of Moore's Law, the evolution towards non-planar device structures, and the resulting steep increase in chip fabrication costs of advanced technologies have given EUROPRACTICE a very important role in the research activities of MICAS. Also, because more and more companies are following a fabless business model, the need for external chip fabrication services is greater than ever for an IC research group like MICAS. Indeed, while a research collaboration with one of the few remaining IDMs can still rely on processing capacity of the fabs of that company, most of the MICAS research partners are making use of the foundry model. For the very small volumes that are typical for a research chip, the only option is to go through EUROPRACTICE.

Some figures about the use of EUROPRACTICE at MICAS

To illustrate how important EUROPRACTICE is in the activities of MICAS, let's look at some numbers of the past year. In 2023, MICAS did 11 tape-outs, with 23 different chip designs, with a combined area of almost 60 mm². A little bit more than 40 mm² of that area was processed through EUROPRACTICE. This means that two-thirds of the total chip area designed by MICAS researchers is realized thanks to EUROPRACTICE. Various technologies have been used, mostly those offered by TSMC, but also specialty technologies like the XFAB 0.18 μm HV SOI technology. Interesting to note is that a very significant portion was processed in TSMC 16 nm CMOS FinFET.

MICAS has a broad research scope in the chip design domain. Its activities go from analog to digital, from DC to terahertz, from oscillators to neural network processors. This results in a myriad of different circuit designs. In the remainder of this article, we will show some remarkable circuits, with special attention to the most extreme circuit properties, demonstrating the wide range of design activities of MICAS. EUROPRACTICE plays an essential role in the realization of these circuits.

From one to millions of transistors

For example, let's look at the number of transistors on a chip. In the research group of prof. Patrick Reynaert, fully CMOS integrated terahertz imaging circuit design is a prominent research topic. In one of the first steps of this research journey, a CMOS terahertz receiver has been implemented[1]. The design contains only one transistor, but it is doing its job at a staggering frequency of 1.06 THz (Figure 1). Based on this receiver, MICAS has already demonstrated terahertz imaging arrays, also fully CMOS integrated.
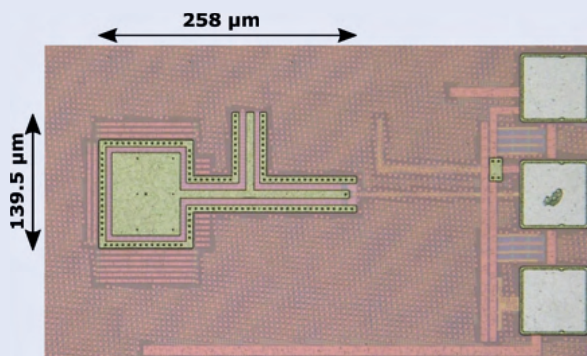

Fig.1: Micrograph of the CMOS terahertz receiver.

At the other side of the spectrum of transistor count, we find digital processors like the DIANA chip (see Figure 2), an end-to-end hybrid digital and analog neural network SoC [2]. Designed in the group of prof. Marian Verhelst, the design is composed of a RISC-V CPU and two deep neural network accelerators: a fully digital array of 16 × 16 processing elements, and a second co-processor based on an analog in-memory compute macro, complemented by a hierarchical distributed memory system and network-on-chip. All in all, the chip contains more than 1 MB of embedded memory and more than 1 million gates.
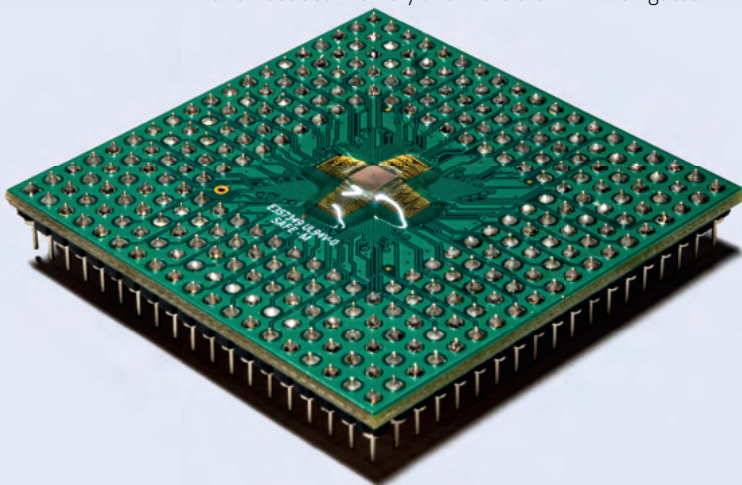

Fig.2: Photograph of the packaged DIANA chip.

From high to low voltage

There is not only a large variety in number of transistors in the designs of MICAS, but also in the voltage range that needs to be handled, be it very high, or very low. In a design of a DC-DC converter [3], realized in the research group of prof. Filip Tavernier, a fully CMOS integrated solution is presented that converts 400 V to 12 V, with an extremely high-power density of more than 100 mW/mm² (Figure 3).
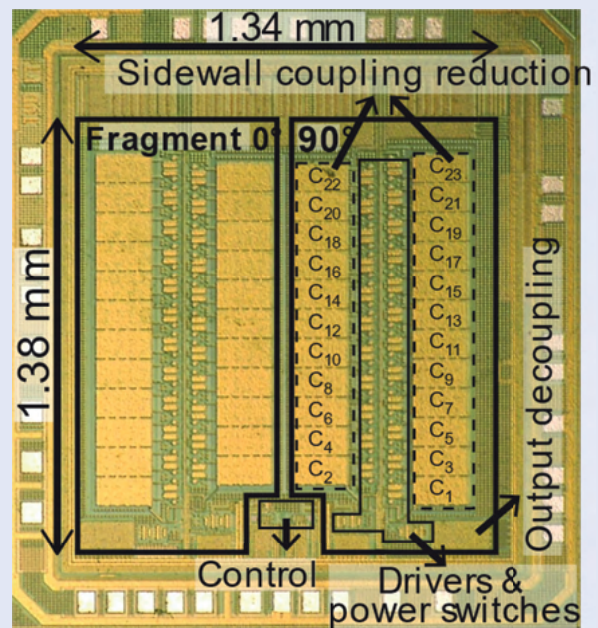
Fig.3: Micrograph of the fabricated DC-DC converter.

On the other hand, in the group of prof. Wim Dehaene, research is being performed on circuits that operate at near-threshold supply voltages. For example, a novel error detection and correction (EDaC) technique has been presented for near-/sub-threshold operation to recover energy lost in the conventional signoff margins [4]. Implemented in a Coolflux DSP, the design achieves a minimum energy point (MEP) of 8.1 pJ/cycle at 0.34 V and 10 MHz, while only adding a 2.8% and 2.1% area overhead for the detection and correction, respectively (see Figure 4).

Low, lower, cryo

We can also look at extremely low temperatures. The design of optimized low-power cryogenic chips depends heavily on an accurate transistor model. Unfortunately, the foundry models that are commonly used are not valid at cryogenic temperatures, resulting in failing chips or in the need for overdesign. Therefore, MICAS has developed its own custom cryogenic transistor model. It is based on accurate transistor

Fig.4: Photo of the Coolflux DSP with integrated EDaC.

measurements on specifically designed test chips containing numerous transistors for cryogenic characterization at 4 K. Figure 5 shows such a test chip.

Fig.5: MICAS' custom cryogenic transistor model test chip.

Extreme environments

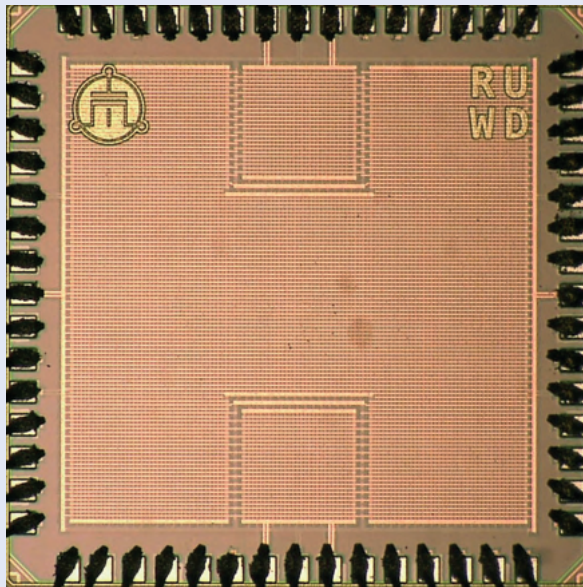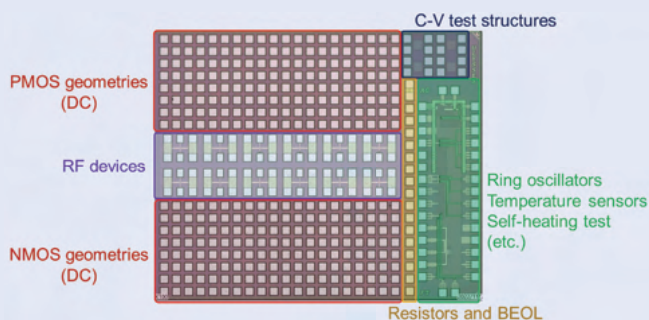Finally, the chips that are designed at MICAS find their way to the most diverse application domains and environments. One of the most striking examples is a chip that acts as the monolithically integrated control unit of a medical device that is implanted into abnormal brain cavities [5]. These are cavities in the brain that are formed as a result of a stroke. The purpose of the implanted device is to restore the functionality of the lost brain cells. In the research group of prof. Georges Gielen, a chip for closed-loop neuromodulation (with both monitoring and stimulation) of the brain cavity wall has been designed. The chip contains time-domain conversion using a novel ADC architecture with record figures for area and power per channel (Figure 6).

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More about MICAS

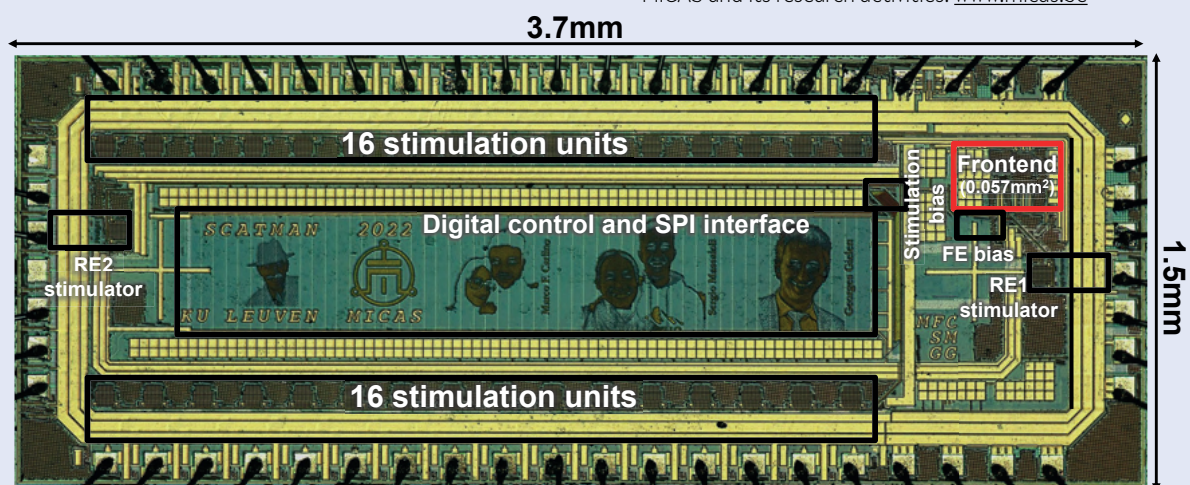MICAS and its research activities: www.micas.be

Fig.6: Photo of the chip for closed-loop neuromodulation of the brain cavity.

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EUROPRACTICE MEMBERSHIP

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R22260	Helmholtz-Zentrum hereon
A13600	Helmut-Schmidt-Universität / Universität der Bundeswehr
A37880	Hochschule Aalen
A12270	Hochschule Albstadt-Sigmaringen
A35710	Hochschule Augsburg
A00670	Hochschule Bremen
A38030	Hochschule Darmstadt
A37450	Hochschule Esslingen
A37240	Hochschule Furtwangen
A15230	Hochschule für Angewandte Wissenschaften Hamburg
A37510	Hochschule für Angewandte Wissenschaften München
R21260	Hochschule für Technik und Wirtschaft Dresden
A15710	Hochschule Hamm-Lippstadt
A38010	Hochschule Heilbronn
A39070	Hochschule Karlsruhe - University of Applied Sciences
A37930	Hochschule Mannheim
A37800	Hochschule Offenburg
A39580	Hochschule Osnabrück
A37920	Hochschule Ravensburg-Weingarten
A39330	Hochschule Reutlingen
A15500	Hochschule RheinMain
A15840	Hochschule Rosenheim
A16330	Hochschule Hannover
A00510	Hochschule Konstanz für Technik, Wirtschaft und Gestaltung
A37530	Humboldt-Universität zu Berlin
R20510	IHP GmbH - Leibniz-Institut für innovative Mikroelektronik
R20300	Institut für Mikroelektronik- und Mechatronik - Systeme gemeinnützige GmbH
R22670	Institut für Mikroelektronik Stuttgart
R20460	Institut für Mobil- und Satellitenfunktechnik GmbH
A16590	IUBH University of Applied Sciences
A35590	Johannes-Wolfgang-Goethe-Universität Frankfurt am Main
A00110	Johannes Gutenberg Universität Mainz

A00850	Justus Liebig-Universität Gießen
A35430	Karlsruher Institut für Technologie
A37290	Leibniz Universität Hannover
A15660	Ludwig-Maximilians-Universiaët München
A39340	Martin-Luther-Universität Halle-Wittenberg
R21050	Max-Planck-Institut für Chemie
R21120	Max-Planck-Institut für extraterrestrische Physik
R22500	Max-Planck-Institut für Mikrostrukturphysik
R00150	Max-Planck-Institut für Physik
R21900	Max-Planck-Institut für Radioastronomie
R22650	Max-Planck-Institute for Software Systems
R21790	NaMLab gGmbH
R22340	Optotransmitter-Umweltschutz-Technologie e.V
A38550	Ostfalia Hochschule für angewandte Wissenschaften
A38090	Otto-von-Guericke-Universität Magdeburg
R22110	Physikalisch-Technische Bundesanstalt - Berlin
R21150	Physikalisch-Technische Bundesanstalt - Braunschweig
R21970	PNSensor gGmbH
A38890	Rheinische Friedrich-Wilhelms-Universität Bonn
A35810	Rheinland-Pfälzische Technische Universität Kaiserslautern-Landau
A38080	Ruhr-Universität Bochum
A39250	Ruprecht-Karls-Universität Heidelberg - ASIC
A16890	Rheinisch-Westfälische Technische Hochschule Aachen - Chair for Distributed Signal Processing
A37810	Rheinisch-Westfälische Technische Hochschule Aachen - Fakultät für Elektrotechnik und Informationstechnik
A16030	Rheinisch-Westfälische Technische Hochschule Aachen - Lehrstuhl für Integrierte Photonik (IPH)
A16040	Rheinisch-Westfälische Technische Hochschule Aachen - Institut für Stromrichtertechnik und Elektrische Antriebe (ISEA)
A16060	Rheinisch-Westfälische Technische Hochschule Aachen - Institut für Theoretische Elektrotechnik (ITHE)
A16320	RWTH Aachen, Physikalisches Institut B
A13680	Technische Hochschule Aschaffenburg
A16680	Technische Hochschule Lübeck
A15410	Technische Hochschule Mittelhessen - Friedberg
A39000	Technische Hochschule Mittelhessen - Gießen
A35400	Technische Hochschule Ulm
A37310	Technische Universität Berlin
A13890	Technische Universität Berlin - Institut für Technische Informatik und Mikroelektronik (TIME)
A35600	Technische Universität Carolo-Wilhelmina zu Braunschweig
A38340	Technische Universität Chemnitz
A35450	Technische Universität Darmstadt - Integrierte Elektronische Systeme (IES)
A37090	Technische Universität Dortmund
A37760	Technische Universität Dresden
A35320	Technische Universität Hamburg-Harburg
A38240	Technische Universität Ilmenau
A37390	Technische Universität München - Fakultät für Elektrotechnik und Informationstechnik München
A12140	Technische Universität München - Fakultät für Physik (Garching)
A16310	Technische Universität Bergakademie Freiberg
A15030	Universität Bielefeld
A13660	Universität Bremen - Informatik
A35620	Universität Bremen - Institut für Theoretische Elektrotechnik und Mikroelektronik
A37440	Universität der Bundeswehr München
A36440	Universität des Saarlandes
A35990	Universität Duisburg-Essen
A35830	Universität Hamburg
A14740	Universität Kassel
A14310	Universität Kassel - Fachbereich Elektrotechnik/Informatik
A16450	Universität Mannheim

A16520	Universität Münster
A37500	Universität Paderborn
A12900	Universität Potsdam
A39220	Universität Rostock
A38220	Universität Siegen
A39110	Universität Stuttgart
A37540	Universität Ulm
A39770	Universität zu Lübeck
A16640	University of Applied Science Nordhausen
A13060	University of Freiburg
A16650	University of Passau
A16090	Westfälische Hochschule
R21770	Konrad-Zuse-Zentrum für Informationstechnik Berlin

Ghana

A14770	Kwame Nkrumah University of Science & Technology

Greece

A39280	Aristotle University of Thessaloniki
R22640	Athena Research Centre
A14150	Athens University of Economics and Business
R20790	Demokritos, National Center for Scientific Research
R21080	Foundation for Research and Technology Hellas
A37550	National and Kapodistrian University of Athens
A35140	National Technical University of Athens
A39490	Technical University of Crete
A16720	National and Kapodistrian University of Athens
A00530	University of Ioannina
A37680	University of Patras
A35960	University of Patras - Electrical and Computer Engineering
A14700	University of Piraeus
A16850	University of the Peloponnese
A13550	University of Thessaly

Hungary

A40010	Budapesti Muszaki és Gazdaságtudományi Egyetem
A47540	Pázmány Péter Katolikus Egyetem

Ireland

A13410	Institute of Technology, Carlow
A01190	Munster Technological University
A13440	National University of Ireland Maynooth
A39310	Technological University Dublin, Tallaght Campus
A36490	Trinity College Dublin
R21720	Tyndall National Institute
A35300	University College Cork
A15730	University College Dublin
A36510	University of Limerick

Israel

A13920	Bar-Ilan University
A13910	Ben-Gurion University of the Negev
A14690	Holon Institute of Technology
A15190	Jerusalem College of Technology
A14540	Kinneret College on the Sea of Galilee
A14070	Ort Braude College of Engineering
A13330	Technion - Israel Institute of Technology
A14380	Tel-Aviv University
A13240	The Hebrew University of Jerusalem

Italy

A16570	University of Bologna
R22550	Consorzio Nazionale Interuniversitario per le Telecomunicazioni
R20550	Elettra-Sincrotrone Trieste
R22450	European Gravitational Observatory
R00140	Fondazione Bruno Kessler
R21940	The Abdus Salam International Centre for Theoretical Physics

R21760	Consiglio Nazionale delle Richerche, Istituto per la Microelettronica e i Microsistemi Catania
R21800	Consiglio Nazionale delle Richerche, Istituto per la Microelettronica e i Microsistemi Roma
R22010	Istituto Nazionale di Astrofisica Osservatorio Astronomico di Cagliari
R22120	Istituto Nazionale di Astrofisica - Istituto di Radioastronomia - Radiotelescopi di Medicina
R21570	Istituto Nazionale di Astrofisica, Istituto di Radioastronomia
R21160	Istituto Nazionale di Astrofisica, Osservatorio Astrofisico di Arcetri
R22490	Istituto Nazionale di Fisica Nucleare
R21190	Istituto Nazionale di Fisica Nucleare, Laboratori Nazionali del Gran Sasso
R20450	Istituto Nazionale di Fisica Nucleare, Laboratori Nazionali di Frascati
R20710	Istituto Nazionale di Fisica Nucleare, Sezione di Bari
R20400	Istituto Nazionale di Fisica Nucleare, Sezione di Bologna
R20670	Istituto Nazionale di Fisica Nucleare, Sezione di Cagliari
R22410	Instituto Nazionale di Fisica Nucleare Sezione di Catania
R20990	Istituto Nazionale di Fisica Nucleare, Sezione di Ferrara
R00270	Istituto Nazionale di Fisica Nucleare, Sezione di Genova
R20630	Istituto Nazionale di Fisica Nucleare, Sezione di Milano
R21100	Istituto Nazionale di Fisica Nucleare, Sezione di Napoli
R20470	Istituto Nazionale di Fisica Nucleare, Sezione di Padova
R21450	Istituto Nazionale di Fisica Nucleare, Sezione di Pavia
R22390	Instituto Nazionale di Fisica Nucleare Sezione di Perugia
R00300	Istituto Nazionale di Fisica Nucleare, Sezione di Pisa
R20310	Istituto Nazionale di Fisica Nucleare, Sezione di Roma
R20320	Istituto Nazionale di Fisica Nucleare, Sezione di Roma II
R20440	Istituto Nazionale di Fisica Nucleare, Sezione di Torino
R20420	Istituto Nazionale di Fisica Nucleare, Sezione di Trieste
R22790	Instituto Nanoscienze - CNR
R22070	Instituto per lo Studio dei Materiali Nanostrutturati
R21600	Istituto Italiano di Technologia
A38380	Politecnico di Bari
A16460	Politecnico di Bari
A35690	Politecnico di Milano
A35530	Politecnico di Torino
R22200	Radio Analog Micro Electronics srl
A15070	Scuola Superiore di Studi Universitari e di Perfezionamento Sant'Anna
A39410	Università degli Studi dell'Aquila
A12990	Università degli Studi di Bergamo
A12390	Università degli Studi di Brescia
A39570	Università degli Studi di Cagliari
A15750	Università Degli Studi di Cassino e del Lazio Meridionale
A37460	Università degli Studi di Catania
A39550	Università degli Studi di Firenze
A35910	Università degli Studi di Genova
A12640	Università degli Studi di Milano
A14800	Università degli Studi di Milano-Bicocca
A12370	Università degli Studi di Napoli Federico II - DIETI
A39200	Università degli Studi di Padova
A35210	Università degli Studi di Parma
A37280	Università degli Studi di Pavia
A00740	Università degli Studi di Perugia
A38840	Università degli Studi di Roma "La Sapienza"
A35550	Università degli Studi di Roma Tor Vergata
A14820	Università degli Studi di Salerno
A00560	Università degli Studi di Siena
A38620	Università degli Studi di Torino
A14220	Università degli Studi di Trento
A13280	Università degli Studi di Udine

A12530	Università degli Studi di Verona
A16130	Università degli Studi Roma Tre
A12770	Università del Salento
A00680	Università della Calabria
A36380	Università di Bologna - Department of Electrical, Electronic, and Information Engineering "Guglielmo Marconi" (Bologna)
A12000	Università di Bologna - DEIS
A00520	Università degli Studi di Modena e Reggio Emilia - Modena
A14860	Università degli Studi di Modena e Reggio Emilia - Reggio Emilia
A35660	Università di Pisa
A00120	Università Politecnica delle Marche

Jordan

A16140	Jordan University of Science & Technology
A15990	Princess Sumaya University for Technology

Kazakhstan

A48080	Nazarbayev University

Latvia

A48060	Riga Technical University

Lebanon

A47650	American University of Beirut

Lithuania

R49200	Baltic Institute of Advanced Technology (BPTI)
R49240	State Research Institute Center for Physical Sciences and Technology
A40230	Kauno Technologijos Universitetas
A48050	Vilniaus Gedimino Technikos Universitetas
A47980	Vilniaus Universitetas

Luxembourg

A15780	Université du Luxembourg

Malta

A38720	L-Università ta' Malta

Moldova

A48000	Universitatea Tehnica a Moldovei

Norway

A37560	Norges Teknisk Naturvitenskapelige Universitet - Institutt for elektroniske systemer
R21460	SINTEF Stiftelsen for industriell og teknisk forskning
A37820	Universitetet i Bergen
A37360	Universitetet i Oslo
A12750	Universitetet i Sørøst-Norge

Palestine

A16370	An-Najah National University
A16240	Birzeit University

Poland

A48270	University Wroclaw
A40140	Akademia Górniczo-Hutnicza im. Stanislawa Staszica
R49080	Centrum Badan Kosmicznych PAN
R49030	Instytut Podstawowych Problemów Techniki PAN (IPPT-PAN)
A47300	Politechnika Gdanska
A47740	Politechnika Lódzka - Pólprzewodnikowych I Optoelektronicznych
A40130	Politechnika Lódzka - Mikroelektroniki I Technik Informatycznych (DMCS)
A47400	Politechnika Poznanska - Inzynierii Komputerowej
A47670	Politechnika Poznanska - Radiokomunikacji
A48230	Politechnika Rzeszówska im. Ignacego Lukasiewicza
A40530	Politechnika Slaska
A40120	Politechnika Warszawska
A40160	Politechnika Wroclawska

R40030	Siec Badawcza Lukasiewicz - Instytut Mikroelektroniki I Fotoniki
R22610	Institute of High Pressure Physics (UNIPRESS)
A40100	Uniwersytet Zielonogórski
A47580	Wojskowej Akademii Technicznej

Portugal

A37230	Instituto de Engenharia de Sistemas e Computadores - Investigação e Desenvolvimento
R22170	Instituto de Sistemas Robótica (ISR-UC)
R21890	Instituto de Telecomunicações - Aveiro
R14120	Instituto de Telecomunicações - Lisboa
A13710	Instituto Superior de Engenharia de Lisboa
A35970	Instituto Superior Técnico
R21750	International Iberian Nanotechnology Laboratory
R21710	Laboratório de Instrumentação e Física Experimental de Partículas
A35670	Universidade de Aveiro
A12550	Universidade do Minho
A35540	Universidade do Porto
A12310	Universidade Nova de Lisboa

Romania

R49010	Institutul National pentru Fizica si Inginerie Nucleara - Horia Hulubei - Nuclear Hadrons
R49060	Institutul National pentru Fizica si Inginerie Nucleara - Horia Hulubei - Particle Physics
A47880	Universitatea Politehnica din Timişoara
A15560	Universitatea Tehnică "Gheorghe Asachi" din Iaşi
A48070	Universitatea Tehnica din Cluj-Napoca
A16070	Universitatea Transilvania Brasov
A15520	Universitatea Nationala de Stiinta si Tehnologie Politehnica Bucuresti

Serbia

R49230	BioSense Institute
R49250	Institute of Physics Belgrade, University of Belgrade
A48010	Univerzitet u Beogradu
A48170	Univerzitet u Kragujevcu
A47510	Univerzitet u Nišu
A48200	Univerzitet u Novom Sadu
A47600	Univerzitet u Novom Sadu

Slovakia

A40050	Slovenská technická univerzita v Bratislave
A47930	Technická univerzita v Kosiciach

Slovenia

A47690	Institut "Jozef Stefan"
R22580	Skylabs Vesoljske Tehnologije Doo
A48260	Univerza v Ljubljani
A40280	Univerza v Ljubljani
A47820	Univerza v Mariboru
A48240	Univerza v Novi Gorici

South Africa

A16930	University of Cape Town (UCT)
A14560	University of Pretoria

Spain

R22470	Asociacion Centro Tecnológico
R22890	Centro Nacional de Aceleradores
R22100	Centro Nacional de Supercomputación, Barcelona
R22880	CIC nanoGUNE
R21740	Centro de Investigaciones Energéticas, Medioambientales y Tecnológicas
R00060	CNM - Instituto de Microelectrónica de Barcelona
R22460	Consorcio ESS Bilbao
R21910	Instituto de Tecnologías Físicas y de la Información

R22600	Centro Tecnológico de Automoción de Galicia
R20700	Ikerlan
R21550	Institut de Ciències Fotòniques
R22750	Institut De Fisica D'Altes Energies (IFAE)
R21520	Institute of Space Sciences (ICE-CSIC)
R22700	Instituto de Astrofísica de Canarias
R21230	Instituto de Fisica Corpuscular
R22870	Instituto Tecnologico de Aragon - ITAINNOVA
A39540	Universidad Carlos III de Madrid
A37330	Universidad Complutense de Madrid
A13340	Universidad de Alcalá
A35891	Universidad de Cantabria
A12590	Universidad de Castilla - La Mancha
A15370	Universidad de Deusto
A39080	Universidad de Extremadura
A38590	Universidad de Granada
A14720	Universidad de La Laguna
A38780	Universidad de Las Palmas de Gran Canaria - Departamento de Informàtica y Sistemas
A36390	Universidad de Las Palmas de Gran Canaria - Instituto Universitario de Microelectrónica Aplicada (IUMA)
A37580	Universidad de Malaga
A38600	Universidad de Navarra
A13860	Universidad de Salamanca
A37080	Universidad de Santiago de Compostela
A38580	Universidad de Sevilla - Ingenieria Electronica
A35870	Universidad de Sevilla - Instituto de Microelectrónica de Sevilla (IMSE-CNM)
A38330	Universidad de Vigo
A37060	Universidad de Zaragoza - Dpto.Ingenieria Electronica y Comunicaciones
A38790	Universidad de Zaragoza - Facultad de Ciencias
A37690	Universidad del Pais Vasco
A12320	Universidad Politécnica de Cartagena
A38820	Universidad Politécnica de Madrid - Centro de Electrónica Industrial
A35130	Universidad Politécnica de Madrid - Departamento de Ingeniería Electrónica
A39100	Universidad Pública de Navarra
A36250	Universitat Autònoma de Barcelona
A39390	Universitat Autónoma de Madrid
A38660	Universitat de Barcelona
A38360	Universitat de les Illes Balears
A13150	Universitat de València
A15100	Universitat Politècnica de Catalunya - Manresa
A35190	Universitat Politècnica de València
A16290	Universitat Pompeu Fabra
A39180	Universitat Rovira i Virgili
A16340	University of Vigo - AtlanTTic
A39150	Universitat Politècnica de Catalunya - Departamento de Ingeniería Electrónica (Campus Nord)

🇸🇪 Sweden

R22930	Center for Bionics and Pain Research
A38670	Chalmers Tekniska högskola
R21990	European Spallation Source
R22050	Institutet för Rymdfysik
A16860	Karlstads universitet
A16360	Kungliga Tekniska Hogskolan, Stockholm
A38180	Kungliga Tekniska högskola, Kista
A37350	Linköpings universitet
A16730	Linnéuniversitetet
A00260	Luleå tekniska universitet
A37370	Lunds universitet
A39840	Mittuniversitetet

R20690	RISE Research Institutes of Sweden AB
R20910	Totalförsvarets forskningsinstitut FOI
A16960	Umeå universitet
A16760	Uppsala universitet
A13720	Uppsala universitet

🇨🇭 Switzerland

R22960	Kantonsspital Baselland Bruderholz
A38410	Berner Fachhochschule
R20350	Organisation Européenne pour la Recherche Nucléaire
R20680	Centre Suisse d'Electronique et Microtechnique - Neuchâtel
R20970	Centre Suisse d'Electronique et Microtechnique - Zürich
A36110	École Polytechnique Fédérale de Lausanne - Microelectronics Systems
A37340	École Polytechnique Fédérale de Lausanne - Neuchâtel
A38800	Eidgenössische Technische Hochschule Zürich - Basel
A38310	Eidgenössische Technische Hochschule Zürich
A14780	Haute école d'ingénierie et d'architecture Fribourg
A38100	Ostschweizer Fachhochschule
R20800	Paul Scherrer Institut
A05000	Scuola Universitaria Professionale della Svizzera Italiana
A13090	Università della Svizzera Italiana
A15480	Universität Basel
A15530	Universität Bern
A16440	Universität Zurich
A13630	Université de Genève
A39820	University of Applied Sciences and Arts Northwestern Switzerland

🇳🇱 The Netherlands

A15420	Erasmus Universitair Medisch Centrum Rotterdam
R20430	European Space Agency - ESTEC Microelectronics
R20540	European Space Agency - ESTEC Payload Technology
R00280	Nikhef
R20520	Stichting Nederlandse Wetenschappelijk Onderzoek Instituten / Stichting ASTRON, Netherlands Institute for Radio Astronomy
R21250	NWO-I/SRON
A12650	Radboud Universiteit Nijmegen
A14510	Rijksuniversiteit Groningen
R21200	Stichting imec Nederland
A13730	Stichting Saxion
A35701	Technische Universiteit Delft
A38050	Technische Universiteit Eindhoven
R20370	TNO-FEL
A16770	Universiteit Leiden
A00170	Universiteit Twente - CAES
A15960	Universiteit van Amsterdam
A12010	Vrije Universiteit Amsterdam

🇹🇳 Tunisia

R22570	Center for Research in Microelectronics and Nanotechnology
A12930	École Nationale d'ingénieurs de Sfax
A15300	École Nationale d'ingénieurs de Tunis

🇹🇷 Turkey

A15680	Ankara Yildirim Beyazit Üniversitesi
A16660	Atilim University
A39170	Bogaziçi Üniversitesi
A16750	Gebze Teknik Üniversitesi
A38270	Ihsan Dogramaci Bilkent Üniversitesi
A15870	Istanbul Bilgi Üniversitesi
A16250	Istanbul Medipol Üniversitesi
A37960	Istanbul Teknik Üniversitesi

A13820	Koc Universitesi
A16550	Maltepe University
A38440	Orta Dogu Teknik Üniversitesi
A15280	Orta Dogu Teknik Üniversitesi Kuzey Kibris Kampusu
A15970	Özyegin Üniversitesi
A13010	Sabanci Üniversitesi
A13530	TC Kocaeli Üniversitesi
A14730	TOBB Ekonomi ve Teknoloji Üniversitesi
R22740	TUBITAK - UME (National Metrology Institute of Turkey)
R38860	Türkiye Bilimsel ve Teknik Arastirma Kurumu -BILGEM
A14250	Yeditepe Üniversitesi
A13950	Yildiz Teknik Üniversitesi

UK

A36280	Brunel University
A15450	Cardiff University
A15790	City University London
A16000	Coventry University
A16050	Cranfield University
R22090	Culham Centre for Fusion Energy
R20950	Diamond Light Source
A13480	Imperial College London
A13490	King's College London
A36342	Liverpool John Moores University
A38450	Loughborough University
A37900	Manchester Metropolitan University
A35330	Newcastle University
A35520	Northumbria University
A15850	Nottingham Trent University
A37490	Queen's University of Belfast
A13510	Royal Holloway University of London
A35030	Sheffield Hallam University
R20600	STFC Daresbury Laboratory
R00050	STFC Rutherford Appleton Laboratory
R22030	STFC UK Astronomy Technology Centre
A37870	Swansea University
A15390	The Open University
A37730	University of Leeds
A14750	UCL Mullard Space Science Laboratory
A13520	University College London
A12480	University of Bath
A37300	University of Birmingham
A36000	University of Bristol
A35780	University of Cambridge
A16580	University of Chester
A37840	University of Durham
A37420	University of Edinburgh
A35440	University of Essex
A35760	University of Exeter
A39440	University of Glasgow
A37600	University of Hertfordshire
A37400	University of Huddersfield
A35410	University of Hull
A36341	University of Liverpool
A35080	University of Manchester
A13620	University of Manchester Jodrell Bank Observatory
A35180	University of Nottingham
A37320	University of Oxford
A39650	University of Salford
A35470	University of Sheffield
A37780	University of South Wales
A37610	University of Southampton
A36120	University of Strathclyde
A37570	University of Surrey
A35111	University of Sussex

A37430	University of the West of England
A36090	University of Ulster
A37630	University of Warwick
A38810	University of York

Ukraine

A48250	Kyiv Academic University
A47610	National Technical University of Ukraine "Igor Sikorsky Kyiv Polytechnic Institute"

Uzbekistan

A16390	Andizhan State University
A16380	Urganch State University

CONTACT INFORMATION

For **general information or enquiries** about EUROPRACTICE, please contact the project coordination team at imec.

For enquiries about EUROPRACTICE **academic membership, design tools or training courses**, please contact the Microelectronics Support Centre, STFC Rutherford Appleton Laboratory, on:

For enquiries about EUROPRACTICE **smart system integration**, please contact Smart Systems Integration service centre:

Romano Hoofman (general)
Tel: +32 (0) 16 283865

Paul Malisse (operational)
Tel: +32 (0) 16 281272
E-mail: mpc@imec.be

Wendy Fannes (legal)
Tel: +32 (0) 16 281571
E-mail: epsec@imec.be

Mark Willoughby (design tools)
Tel: +44 (0) 1235 445327
E-Mail: MicroelectronicsCentre@stfc.ac.uk

Clive Holmes (training courses)
Tel: +44 (0) 1235 445327
E-Mail: MicroelectronicsCentre@stfc.ac.uk

Richard Bishop (academic membership)
Tel: +44 (0) 1235 445327
E-Mail: MicroelectronicsCentre@stfc.ac.uk

Marc Rensing (general)
Tel: +353 21 234 6613
E-mail: marc.rensing@tyndall.ie

For more specific enquiries concerning **technology access, MPW schedules, and related customer support**, please contact one of the following EUROPRACTICE support centres:

TSMC Technologies
Tobias Vanderhenst
Tel: +32 (0)16 287889
E-mail: eptsmc@imec.be

UMC Technologies
Ahmed Ba-Makhramah
Tel: +32 (0)16 283142
E-mail: epumc@imec.be

X-FAB & MEMS Technologies
Pieter Claes
Tel: +32 (0)16 288770
E-mail: epxfab@imec.be

Si-Photonics Technologies
Mulham Khoder
Tel: +32 (0)16 283655
E-mail: epsiphot@imec.be

GaN-IC Technology
Maritza Tangarife Ortiz
Tel: +32 (0)16 281372
E-mail: ganmpw@imec-int.com

Pragmatic Technologies
Adil Masood
Tel: +32 (0)16 288054
E-mail: flexicmpw@imec-int.com

ams Technologies
Elvira Liandres
Tel: +49 (0)9131 776-4464
E-mail: virtual-asic@iis.fraunhofer.de

GLOBALFOUNDRIES Technologies
Syed Shahnawaz
Tel: +49 (0)9131 776-4425
E-mail: vaf-helpdesk@iis.fraunhofer.de

IHP Technologies
Elvira Liandres
Tel: +49 (0)9131 776-4464
E-mail: virtual-asic@iis.fraunhofer.de

X-FAB Technologies
Ruslan Rybalko
Tel: +49 (0)9131 776-7344
E-mail: vaf-helpdesk@iis.fraunhofer.de

UMS Technologies
Elvira Liandres
Tel: +49 (0)9131 776-4464
E-mail: virtual-asic@iis.fraunhofer.de

ams Technologies
Gaétan Debontride
Tel: +33 4 56 52 94 40
E-mail: cime-prototypage@grenoble-inp.fr

EM Microelectronic Technologies
Gaétan Debontride
Tel: +33 4 56 52 94 40
E-mail: cime-prototypage@grenoble-inp.fr

STMicroelectronics Technologies
Abdelhamid Aitoumeri
Tel: +33 4 56 52 94 20
E-mail: cime-prototypage@grenoble-inp.fr

Science Technologies
Zineb M'Harzi
Tel: +33 4 56 52 94 30
E-mail: cime-prototypage@grenoble-inp.fr

Si-Photonics Technologies
Zineb M'Harzi
Tel: +33 4 56 52 94 30
E-mail: cime-prototypage@grenoble-inp.fr

EUROPRACTICE

SHAKKEI.COM

design & layout:

EUROPRACTICE Consortium Partners:

imec

imec
General EUROPRACTICE-IC office
& IC Manufacturing Centre
Kapeldreef 75
B3001 Leuven, Belgium

UKRI-STFC
Science and Technology Facilities Council

UKRI-STFC
Microelectronics Support Centre –
EUROPRACTICE EDA tools and training office
Rutherford Appleton Laboratory
Didcot, Oxfordshire, OX11 0QX, United Kingdom

Fraunhofer IIS

Fraunhofer IIS
IC Manufacturing Centre
Am Wolfsmantel 33
D91058 Erlangen, Germany

CIME-P

CIME-P
IC Manufacturing Centre
3 parvis Louis Néel CS50257
38016 GRENOBLE Cedex 1, France

Tyndall National Institute

Tyndall National Institute
Smart Systems Integration Service Centre
Maltings Complex Dyke Parade,
Cork, T12 R5CP, Ireland

Chips JU