CHIPLET INTEGRATION SERVICES WITHIN EUROPRACTICE

DESIGN RULES and SERVICE

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Version updated by Photonics Packaging and Systems Integration Group, Tyndall National Institute, EUROPRACTICE Partner

Tyndall National Institute Institiúid Náisiúnta

EUROPRACTICE

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1. Summary

1.1. Objective

The Photonics Packaging Group at the Tyndall National Institute in Ireland is a Europractice partner and offers packaging and integration services for Silicon Photonic Integrated Circuits (Si-PICs) fabricated in the MPW runs. We are aware of the fact that a Europractice MPW run is often the first instance in which a researcher, or SME, ventures into the field of fabricating real integrated photonic devices. This document has been developed as a guide and tutorial to help design chiplets that are compatible with standard integration technologies offered by Tyndall. We strongly encourage users to review this document and design rules, interested in our chiplet integration services.

1.2. Goals

The three goals of this document are

(i) to educate new users on the basic principles and terminology of chiplet integration,
(ii) to help users design chiplets that are compatible with the integration technologies available at Tyndall,
(iii) to list the different chiplet integration options that Tyndall can offer to Europractice users.

To understand system integration and the reasons behind the restrictions and conventions, it is necessary to have a basic familiarity with chiplets, heterogenous integration, electrical packaging and micro-transfer printing. Therefore, we provide a short tutorial on these topics in ***Section 2***. This tutorial also describes the standard package options that Tyndall have developed, which have been designed to enable users to realise low-cost chiplet integrated modules (optical, electrical, and thermal) for their chiplets. The three standard chiplet integration options, integration of electronic-ICs to standard silicon interposers via flipchip bonding and integration of photonic devices (lasers and photodiodes) onto submounts via micro-transfer printing, available to Europractice users (or non-Europractice users wanting compatible system integration services) are given in ***Section 3***. At the end, you can find general information about Tyndall`s new service flow, Multi-Project Chiplet Integration Run (MPP-Run), under Europractice, organized in order to lower the cost barrier for system integration and packaging.

1.3. Glossary

The following are a list of abbreviations frequently used in this document:

AlN : Aluminium nitride

IC : Integrated Circuit

MPW : Multi-Project Wafer

MTP: Micro Transfer Printing

PCB : Printed Circuit Board

PD : Photo Diode

PDMS : Polydimethylsiloxane

PDR : Packaging Design Rules

PIC : Photonic Integrated Circuit

PMF : Polarisation Maintaining Fibre (assumed to also be single-mode)

RDL : Redistribution Line

SEM : Scanning Electron Microscope

SMF : Single Mode Fibre

SOI : Silicon on Insulator

SiO_2 : Silicon dioxide

TEC : Thermoelectric cooler

UTC PD : Uni-Travelling-Carrier Photodiode

2. Tutorial

As the design phase and rule checking takes the longest amount of time during the integration process, it is critical to have standard components to shorten this period. Furthermore, to ensure efficient and reproducible packaging of electronic or photonic components, it is important to standardize their layout so that generic integration solutions and processes can be utilized. Considering these, the Photonic Packaging Group at Tyndall (www.tyndall.ie/packaging) has developed a series of design rules that cover some of the most widely used in assembly and integration technologies.

This section provides a basic overview of the principles of electronic-IC packaging methods like wire-bonding and flip-chip bonding, and micro-transfer printing. It concludes with a description of the heterogeneous integration of:

i) Electronic-ICs onto Tyndall-designed silicon interposers and PCB modules via flip-chip technology, which have been developed to allow users to easily create electrically packaged modules that offer electrical access to their integrated circuits, without requiring a custom designed housing.

ii) Photonic devices (lasers and photodiodes) onto Tyndall-designed silicon submounts via micro-transfer printing, which have been developed to allow users to create electrically and optically packaged modules that offer easy access to their photonic devices, without the need for a custom designed housing.

2.1. Chiplet Definition

A chiplet is a smaller, modular integrated circuit (IC) that functions as part of a larger processor or system-on-chip (SoC). Instead of manufacturing an entire processor or system in one large monolithic die, chiplets allow designers to split the processor into multiple smaller dies, which are then connected together to function as a unified whole. The semiconductor industry is undergoing a significant transition towards chiplet-based designs, driven by the demand for higher performance, greater flexibility, and cost efficiency. These chiplets are integrated into a single package, enhancing flexibility, performance, functionality and cost-effectiveness. However, the challenges associated with the packaging of chiplets is often underestimated and remains technically challenging due to the variety and complexity of the technologies involved, as well as the need for efficient thermal management and power efficiency, combined with the lack of standards available to IC designers. This greatly affects the cost of assembling prototype

chiplet packages and the scalability to volume manufacturing. Considering these challenges, Tyndall has developed new chiplet integration offers based on using standardized components which allows for a wide range of off-the-shelf chiplet integration and avoids the need for new designs at each request. *Error! Reference source not found.* provides an example where multiple chiplets are integrated onto a single interposer, which will subsequently form part of a larger package.

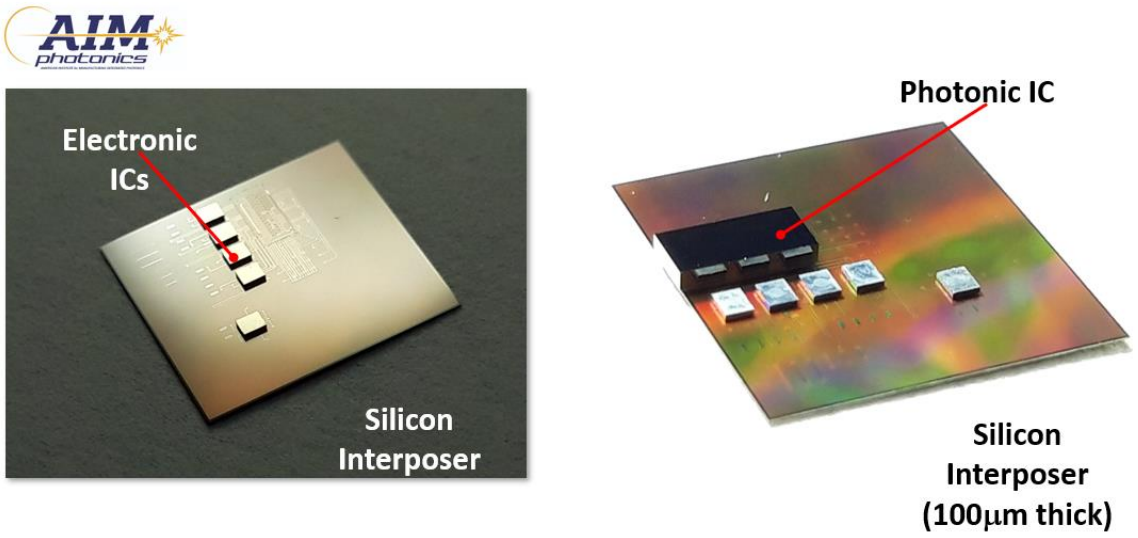

Figure 1. General overview of integration of multiple chips into single package. Five electronic chiplets are combined with a single photonic chiplet on an active silicon interposer.

2.2. Heterogenous Integration

Heterogeneous integration is the process of combining diverse components—such as materials, technologies, or functional units—into a unified system or package to function cohesively. In electronics and semiconductor applications, it involves integrating multiple components like logic, memory, analog circuits, RF (radio frequency) modules, photonics, and sensors, which may utilize different semiconductor processes or materials, onto a shared platform. Heterogeneous integration allows the combination of silicon with other materials such as indium phosphide (InP), germanium (Ge), or gallium arsenide (GaAs) to create photonic devices with enhanced capabilities. This integration enables the development of photonic integrated circuits (PICs) that offer high-speed data transmission, compact form factors, and low power consumption, which are critical for applications in data centers, telecommunications, and quantum computing. Heterogeneous integration also allows for the use of advanced packaging techniques like micro-transfer printing or wafer bonding, ensuring

that different materials can be precisely aligned and connected. This approach not only improves the performance of the system but also offers flexibility in design, reducing the time and cost required for development.

We offer integration and packaging solutions for all silicon dies under Europractice, whether they are made through a Europractice MPW or not, as long as the provided PDRs are followed. We strongly recommend reviewing your design with your chosen packaging partner before submitting it to a foundry. For Europractice System Integration Services, we strongly recommend to contact Tyndall for the design review.

2.3. General Information and Rules for Electrical Packaging

This section summarizes the general principles that are followed at Tyndall for electrical packaging and are available options for Europractice users.

2.3.1. Wire-bonding

Wire bonding is the most common method of providing an electrical connection from an IC to a PCB within a package. To help users access integrated electrical components on their Si-ICs, *Tyndall* provides Au ball wire bonding (DC) as part of the *Europractice* packaging service.

For standard ball bonding, DC bond-pads on the Si-IC must have a minimum pitch of 150µm and may not be staggered - see ***Figure 2***, as staggering bond pads on the PIC increases the likelihood of shorting between adjacent wire bonds. *Tyndall* can make wire-bond connections to all standard bond-pads defined as part of PDKs from the main European foundries (such as those offered by *IMEC* or *CEA-Leti*). If users opt for custom bond-pads, they must have a minimum footprint of 50µm x 70µm. All bond-pads for wire-bonding must have a Au-capping layer that is at least 100nm thick. *Tyndall* uses circular-section 18µm-diameter Au-wire for DC wire-bonds, and 50*µm* x 12*µm* tape-section Au-wire bonds.

It is recommended to keep bonds as close to the chip edge as possible. This ensures that the wire bond length is kept as short as possible when connecting the IC to a PCB. Additionally, it is recommended that bond-pads for electronic-coupling should be located along the North- and South-sides of the die, and cantered with respect to the die, refer to *Error! Reference source not found.* for optimum layout. It is also critical to ensure that bond pad metallisation on the PIC is compatible with the chosen assembly process.

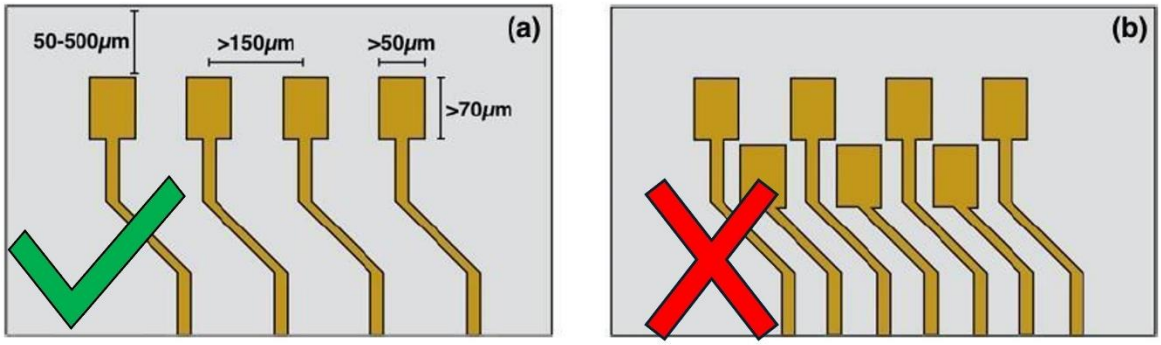

Figure 2. (a) Bond-pads must have a minimum pitch of 150µm, and be located between 50µm and 500µm from the edge of the IC. If users opt for a custom bond-pad design, then the pad must have a minimum footprint of 50µm x 70µm. (b) Staggering of bond-pads is not acceptable for Europractice chiplet integration and packaging.

Table 1 summarizes the acceptable metallisation and main design rules for electrical photonic packaging provided in Europractice. Please note that these design rules are recommendations based on our current standard processes in Europractice.

Table 1. Electrical packaging design rules offered under Europractice

Electrical Packaging Design Rules		
Connection method	Wire bonding (DC)	
Bond pad size	≥75*µm* (minimum)	
Bond pad distance from edge	≥150µm	
Bond pad location on IC	North- and South-sides of, and centered with respect to EIC	
Bond Pad pitch	*≥150µm* (minimum)	
Max no of DC bond pads	120	
Metallisation	Preferred Metal	Acceptable Metal
	Au	Al

2.3.2. Electrical Interposers

Where there is an electro-mechanical mismatch between the ICs and PCB bond pads, electrical interposers are used as intermediate structures to bridge the mismatch between the IC and PCB. These can take the form of thin-film ceramics or Silicon interposers. For 2.5D and 3D integration, flip chip bonding of electrical ICs (or in some cases, PICs) is becoming popular due to its potential for package footprint reduction and improved electrical performance. A variety of different interposer structures can be used depending on the specific application and requirements. These include materials such as glass, ceramic or LTCC.

For DC connections, interposers can also be used to facilitate the packaging of ICs with large numbers (i.e. 200+) of closely spaced electrical contacts which need to be fanned out towards a PCB. These types of interposers can include single level silicon structures are shown in ***Figure 3***. These interposers are typically designed for use with flip chip bonding, which provides a convenient way of electrically interconnecting the IC. One of Tyndall's integration offer relies on this technology. Flip-chip bonding will be described in following section.

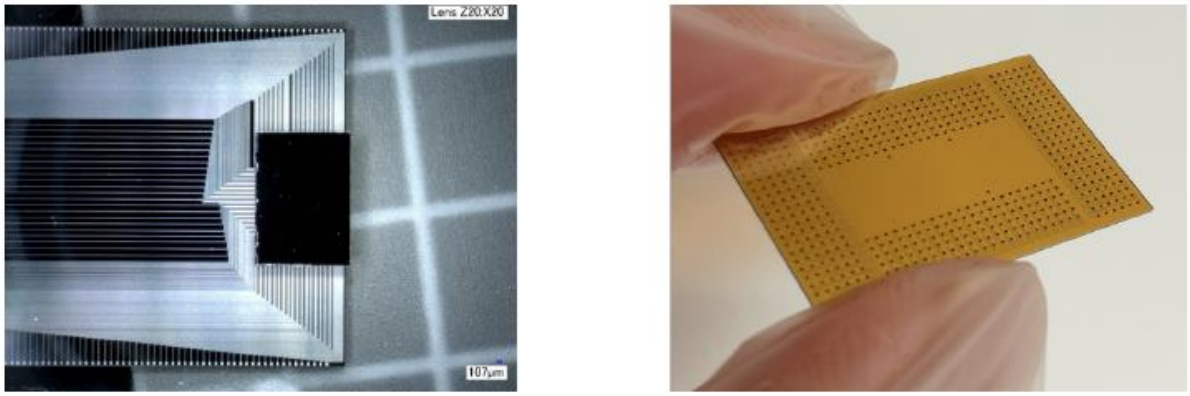

Figure 3. Interposers are used to fan-out electrical connections from a PIC to a PCB or other carrier. (left) Silicon interposer and (right) Glass interposer.

2.3.3. Flip-chip bonding

Flip-chip packaging is a critical, die level, electrical interconnect technology used to achieve high placement accuracy between devices bonded to substrates and interposers. The physical length of electrical connections between devices, such as electronic-ICs to interposer, should be minimized. At Tyndall, using our PacTech Solder Bumper (SB^2) and Finetech Flip Chip system, an EIC can be bonded onto an interposer (or interposer onto a PCB) to reduce the electrical length. This approach can also be useful for EICs with large numbers of electrical connections, where the EIC is bonded to a carrier interposer to fan-out the electrical lines. The general process for flip chip bonding is outlined in ***Figure 4***. The SB^2 can rapidly apply *50µm* solder balls to an extended 2D array of Au-finished bond-pads on the EIC, which are then aligned with respect to their corresponding bond pads on the interposer, using flip chip system. Both are then brought into contact, and electromechanically bonded together by solder re-flow around 250°C. For solder ball-bump and flip chip packaging, the bond pads on the EIC and interposer should both be minimum *50µm* × *50µm* in size and be separated by a a gap of 50µm giving a pitch of at least *100µm*. Always ensure that the bond pad pitch is consistent between both the EIC and the interposer. At Tyndall our system can handle die ranging in size from approximately *300µm* × *300µm* up to a maximum size of 22mm

× 22mm. To ensure good adhesion of the solder ball to the bond-pad, the Au-thickness on the pads should be at least 500nm.

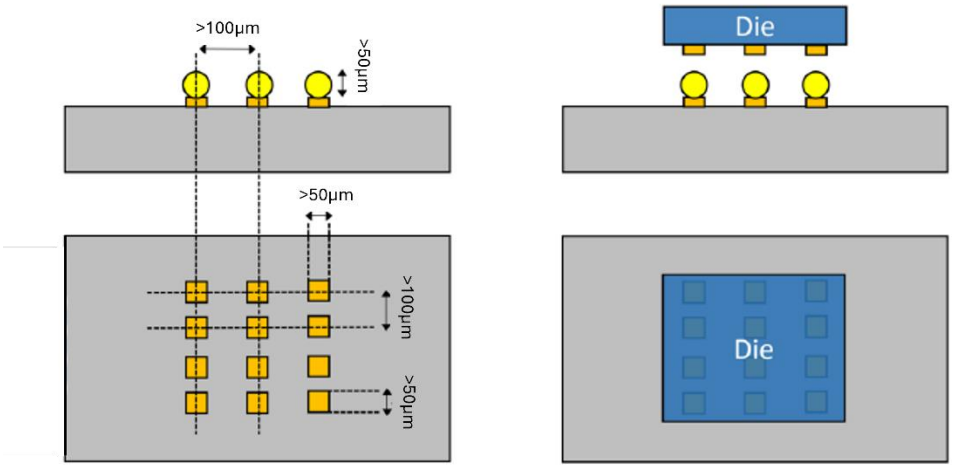

Figure 4. (left) Summary of some general design rules for flip-chip bonding on a PIC. (right) Schematic of EIC which can be flip-chip bonded.

Detailed information about Tyndall's chiplet integration offer onto silicon interposers and their assembly to a customized PCB and mechanical housing is given at ***Section 3.1.*** Electronic-ICs Integration Service

2.4. General Information for Micro-transfer Printing

Micro-transfer printing (MTP) is a cutting-edge technology in heterogeneous integration that enables the transfer of microscale structures and devices from one substrate to another with high precision and accuracy. This process involves the release of the source material to be transferred, the picking of the material (coupons) from the source wafer and the transfer and release (print) of the material to a new substrate (target).

Picking up and transferring of materials are achieved using a stamp, made from the elastomeric material polydimethylsiloxane (PDMS), which can conform to the surface topography of the materials being transferred, thus making the PDMS stamp is central to the MTP technology. PDMS has unusual viscoelastic properties, and the picking and printing mechanism relies on the variable viscoelastic adhesion properties of the stamp. The adhesion of PDMS depends on the separation speed of the PDMS and the material it is in contact with. Briefly, in MTP when the PDMS separation speed is high, its adhesion becomes higher (sticky) allowing the stamp to pick the coupon. When the separation speed is low the adhesion is lower allowing the coupon

to be released from the stamp and print onto the target surface. After each transfer, the stamp is then cleaned and ready to print again. A plot of separation energy as a function of separation speed and the MTP cycle is shown in ***Figure 5***.

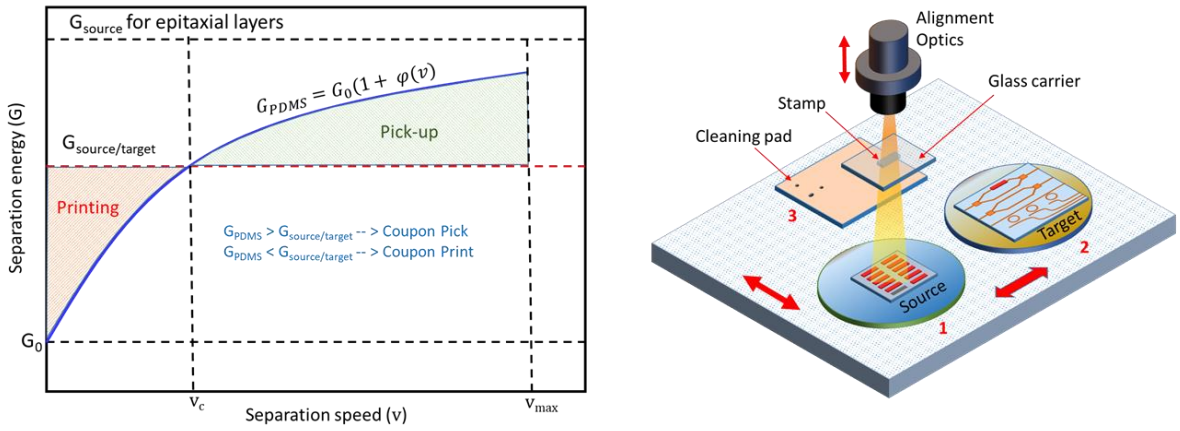

Figure 5. (left) Plot of separation energy as a function of separation speed for PDMS. The MTP cycle 1. Pick 2. Print 3. Stamp Clean

At the core of MTP technology is the controlled release of coupons for transfer printing. This requires a material with a selectively etchable release layer, allowing precise removal from the surface. The material to be transferred is anchored in place by tethers that break during the picking process. The coupon area is defined by lithography and etched to the top of the release layer. Essential layers are protected, and the release layer is etched through. Tethers are placed to secure the coupon in place. A simplified schematic illustrating the generation of MTP coupons is shown in ***Figure 6***.

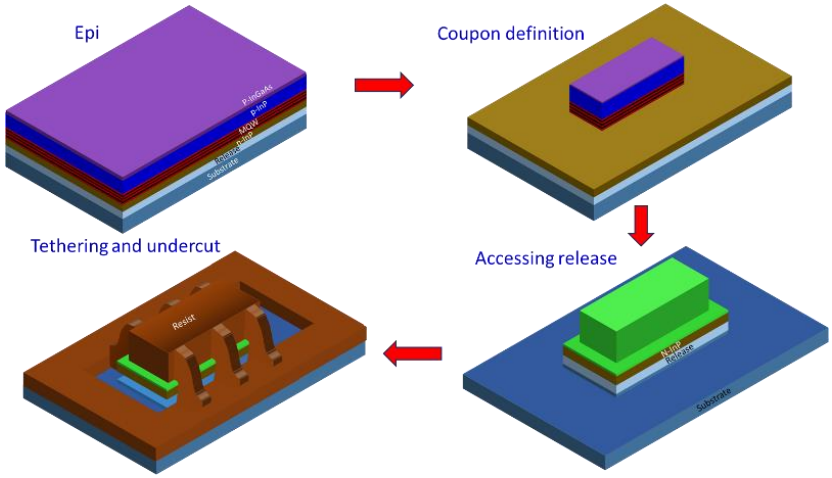

Figure 6. Schematic for the fabrication of MTP coupons

In Europractice, Tyndall offers a range of MTP services for both Si-PICs and other applications. Currently, we offer two active component types for transfer print. Briefly, the first offer being an edge emitting etched facet laser operating at 1550 nm, and the second offer a UTC photodiode capable of high speed operation but for current demonstrations will operate at lower speeds ~ 1 GHz unless custom RDL lines to connect to the device are provided. These would not be included in the general offer for now, but we are planning the implement this in our future offers

Our laser integration includes printing of a single, or an array of four, lasers onto a standardised silicon based submount provided by Tyndall; wirebonding of the printed lasers to the submount for electrical connection; fibre array attachment to the submount for coupling, depending to the user's interest.

Our UTC photodiode integration offers printing of a single, or an array of four, UTC PDs onto a standardised SOI based submount provided by Tyndall. This submount includes grating couplers for input fibre, grating couplers for the PDs and waveguides that connect the two coupler. RDL to electrically connect the PDs to the edge of the chip and provide for electrical contact are established. The chip is then completed with an input fibre coupling array.

Both of MTP service offers can be further packaged and wirebonded onto a larger Tyndall designed PCB to allow for cable out and a larger mechanical structure. The MTP services can accommodate a range of demands from just devices printed to a submount all the way to a fully packaged device with electrical and optical connections, depending on user needs. Whatever option is chosen, we highly recommend carefully following PDR, especially if a custom PIC is provided for MTP services. Detailed information about the device types and services is given ***Section 3.2.*** Micro Transfer Printing Service & Design Rules

3. Heterogenous Integration Services in Europractice

This section describes Tyndall's three different heterogenous integration options available to Europractice users, and how they can be customised to best match their electronic/photonic devices being integrated onto Tyndall designed components and standard modules in order to test and validate their devices.

3.1. Electronic-ICs Integration Service & Design Rules

Below explains the rules and detailed information about electronic chiplet integration service that Tyndall offers for Europractice users.

3.1.1. Die Layout

To use the packaging and assembly services at Tyndall, we suggest designing the electrical interface of your die following the layout in ***Figure 7***. This design allows you to choose from standard integration and packaging options, which are more cost-effective and save development time. The dies have an electrical interface that allows them to be flip-chipped onto a silicon interposer. Currently, Tyndall cannot support Europractice users with RF design assistance or RF packaging. The design guidelines are based only on basic DC connections without RF lines.

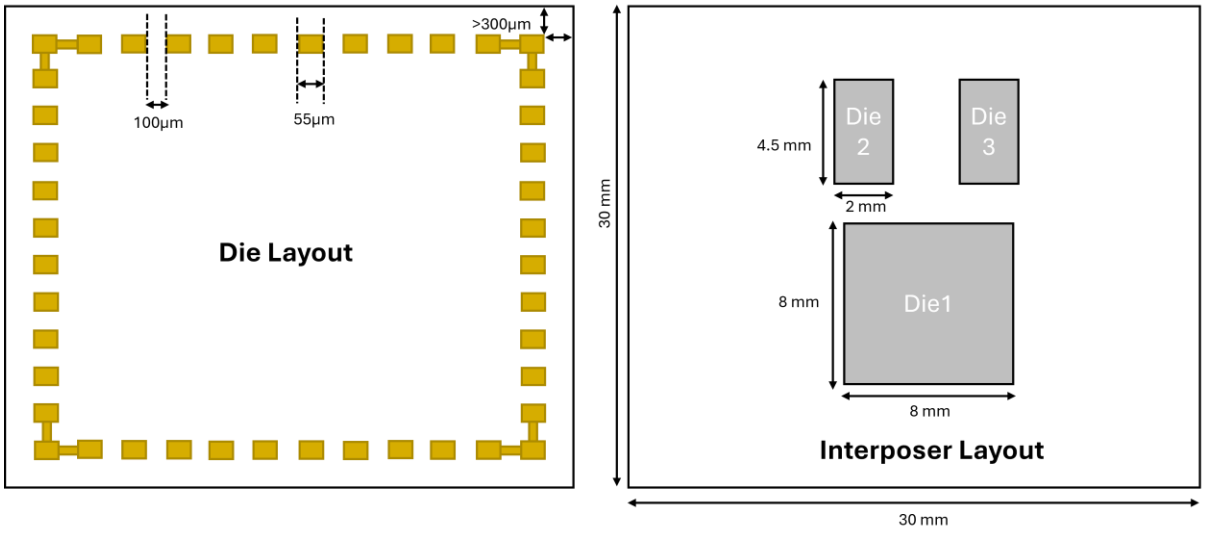

Figure 7. I/O layout for die (left) and an example layout for multiple die on the interposer (right) for integrating/testing chiplets.

For standard ball bonding, DC bond pads (micro bumps) on the dies should typically be at least $55\mu m \times 55\mu m$ in size and separated by a gap of at least $100\mu m$, as shown in ***Figure 7***. All bond

pads should be located at the edge of each IC, with a minimum clearance of more than 300μm from the edge of the die. We recommend against staggering bond pads on the die due to the increased risk of shorting between adjacent DC bond pads. Die sizes ranging from 300µm x 300um up to 20mm x 20mm can be accommodate on the interposer. If possible, users should consider adding a few daisy chain connections on their die to facilitate the verification of electrical connections later on.

If required, Tyndall can provide EIC preparation services such as solder ball jetting of users chips.

3.1.2. Tyndall Designed Silicon Interposer

For Europractice users, Tyndall will initially offer single-layer Redistribution Layer (RDL) metal-based silicon interposers for integrating their electronic chiplets by flip chip bonding.

The wafers are 100 mm silicon wafers with an overall thickness of 525μm, fabricated in Tyndall's cleanroom. The interposer dimensions are fixed at 30 mm × 30 mm and will accommodate as many dies that will fit within this foot-print. ***Figure 8***. Shows an example case of 3 dies**.** A 100 mm wafer produces four 30 mm × 30 mm interposers, and this number is fixed for Europractice services, to keep costs low. The fabrication process utilizes a standard lift-off method with an approximately 1 µm gold layer deposition for the RDL. Each interposer can support up to 260 DC connections. The interposer has 260 square pads, each measuring 250μm × 250μm, arranged along its four edges with a 450μm pitch. Users can request a customized interposer with more or fewer EICs or DC connections, which may affect the cost and delivery time.

The design rules for our interposer design are presented in

Table 2.

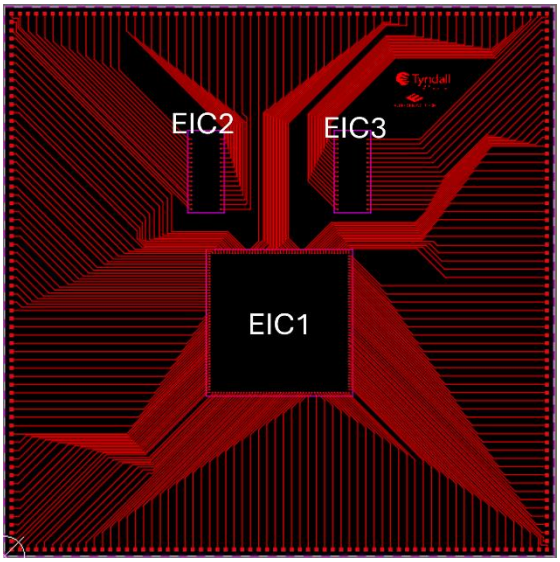

Figure 8. Tyndall designed/fabricated silicon interposer (30mm × 30mm) with given ICs dimensions. The interposer dimension is fixed and standard. The IC dimensions and number of DC connections can be changed, as needed.

Table 2. Design rules for chiplet integration onto Tyndall silicon interposer available for Europractice users

Interposer Design Rules	
Material	Silicon
Size	30 mm × 30 mm
Total DC connections	260
Metallization (Single Layer)	AU
Metallization thickness	1µm
Microbump pad	55µm
C4 bump pad	250µm
Microbump pitch	255µm
C4 bump pitch	450µm
Microbump pitch	255µm
C4 bump pitch	450µm

3.1.3. Tyndall Designed PCB

Printed Circuit Boards (PCBs) are critical components in chiplet integration, providing the mechanical foundation and electrical interconnections for the dies. Designing an efficient and reliable PCB requires adherence to specific design rules and guidelines to ensure functionality, manufacturability, and compliance with industry standards. It is also crucial to choose materials

that approximately match the coefficients of thermal expansion (CTE) of the interposer material with the chiplets.

For Europractice users, Tyndall offers single-sided PCBs with surface-mounted I/O connectors. Tyndall provides four 70-pin flex connectors for the 260 DC connections on the PCB. The PCBs are made of FR4 material and measure 7 cm by 7 cm. Most PCB design rules are based on IPC standards. We also offer aluminium baked and IMS (Insulated Metal Substrate) PCB materials for situations where thermal issues are critical. These PCBs are single-sided with high Tg (Glass Transition Temperature).

3.1.4. Standard chiplet integration via flip-chip bonding

Our approach uses a custom-designed single-layer silicon interposer placed between the various functional dies and a printed circuit board (PCB), forming a 2.5D integration to route multiple DC connections – see ***Figure 9***. To ensure a reliable electrical connection between the dies and the silicon interposer, we utilize a well-established process that involves gold stud bumping and coining on the aluminum bond pads of the dies, followed by flip-chip bonding onto the silicon interposer with 50 µm SAC 305 solder balls. The details of the flip-chip bonding process and the gold stud coining that have been used in Tyndall are given in ***Flip-chip bonding*** section.

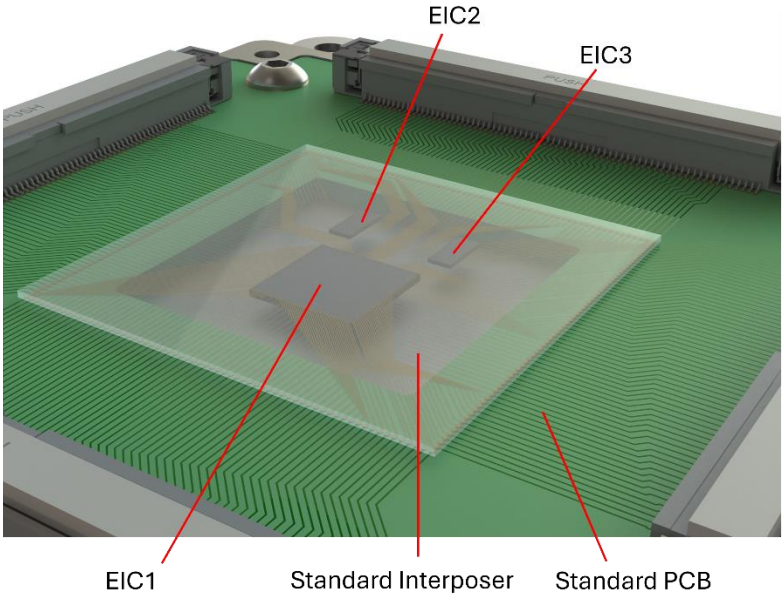

Figure 9. Different dies integration onto Tyndall's standard silicon interposer, and its assembly to Tyndall designed PCB. To make chiplets visible silicon interposer is illustrated in transparent.

For interfacing with external driver circuits, a customized Tyndall generic PCB is designed in such a way that it should perfectly match the bond pads of the layout of the interposer. A flip-chip bonding process is then performed to establish the electrical connection between the interposer and the PCB through the low-melting Bismuth-Tin (Bi-Sn) solder balls. The whole assembly is then mounted on a mechanical base to make a final prototype for the user. ***Figure 10*** illustrates the details of the packaging strategy for seamlessly integrating electrical connections of the die to enable chiplet integration.

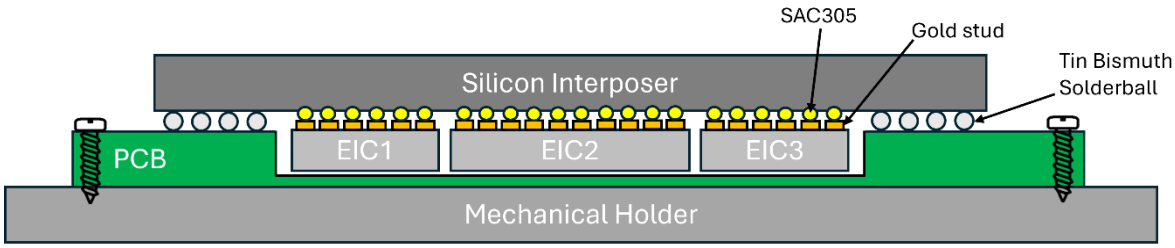

Figure 10. Schematic representation of chiplet integration by flip chip bonding.

3.1.5. Standard package for chiplet integration via flip-chip bonding

For Europractice users, Tyndall provide different packaging options for users ICs, including EIC preparation: dispensing of solder balls, flip-chip bonding of user chips onto Tyndall designed silicon interposer, flip-chip bonding of this interposer to Tyndall PCB, assembly into a packaged module, depending on the user's need. Please note that each provided service will have different pricing depending on the used materials and processes.

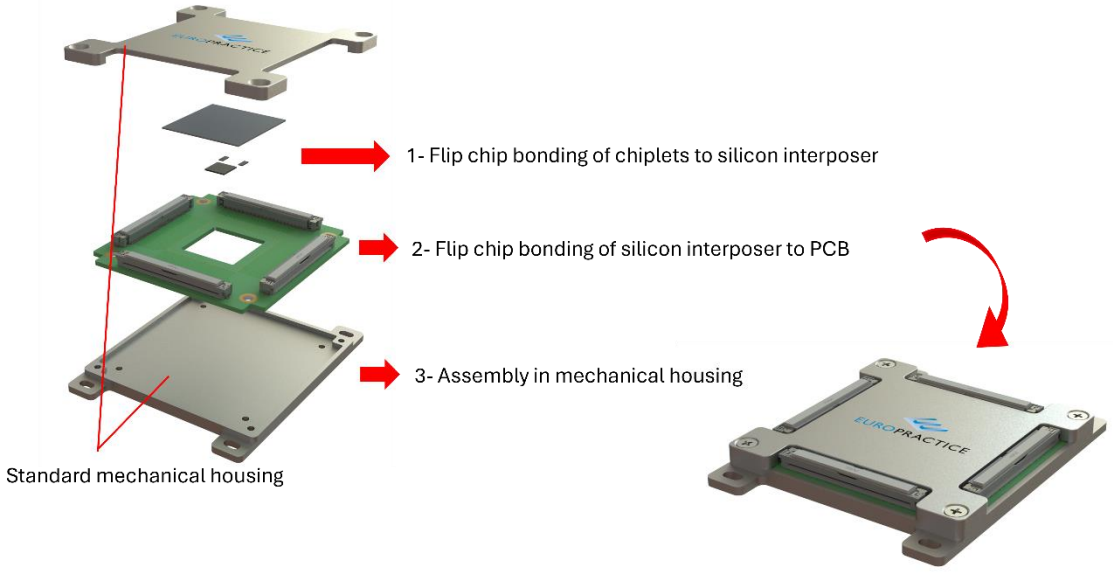

Figure 11. Overview of chiplet integration service options for Europractice users.

In order to provide low-cost solutions for Europractice users, the package components and packaging processes are standardized. As shown above, the interposer dimensions are fixed in order to provide optimum fabrication process, however the maximum number of connections could be reviewed with users if custom solutions are needed. This interposer can accommodate as many ICs as can fit within the 30mm x 30mm footprint. Please note non-standard solutions may cause additional pricing and delivery depending on the fabrication.

Table 3. Summary of the standardized package for chiplet integration for Europractice users

Chiplet Integration – Generic Package Summary	
Electrical connection	2.5D integration – Flip-chip bonding
Connection material chiplet to interposer	Gold stud bumping and coining
Connection material interposer to PCB	low-melting Bismuth-Tin (Bi-Sn)
Interposer material - no. of layer - size	Silicon – single layer – 30 mm × 30 mm
Interposer DC connections	Maximum 260
Number of chiplets	As many as fit on interposer
PCB connections	Maximum 260 – 4 Connectors
Mechanical housing dimensions (with holes)	92 mm × 74 mm × 8.3 mm

3.2. Micro Transfer Printing Service & Design Rules

Below explains the rules and detailed information about photonic components integration through micro transfer printing service that Tyndall offers for Europractice users.

Currently, we offer printing lasers and photodiodes onto submounts, through standardized components and MTP and packaging processes in order to provide low-cost solutions for Europractice users.

3.2.1. Laser Integration Service

Laser integration services for Europractice includes the printing of lasers onto submounts, and their electrical, optical and mechanical assembly to Tyndall designed components in order to provide Europractice users to test their devices.

Below describes the related information and rules in detail.

Tyndall's Laser Coupon Information

Tyndall offers a standard etched facet edge emitting laser for transfer print onto either silicon submounts designed and supplied by Tyndall or user provided substrates or PICs. However,

any user supplied substrates must conform to the integration guidelines and capabilities prior to the service being engaged. The laser coupon is InP based with a maximum thickness of 5.4µm including the laser epitaxy, dielectric coatings, and metal contacts. The mode centre of the laser is located 2.3μm from the base of the laser coupon. The laser threshold current is of the order of 20 mA and the maximum power output is of the order of 10 mW. Typical LIVT characteristics of the laser are shown in ***Figure 12***.

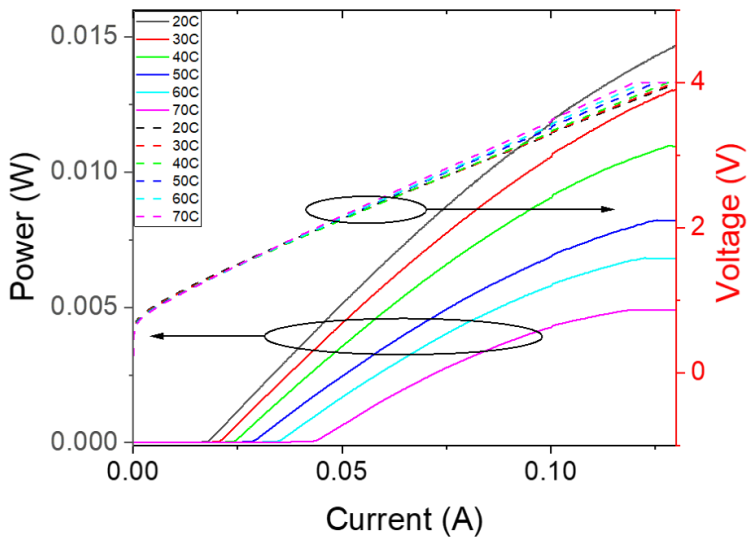

Figure 12. Typical LIVT characteristics of a Tyndall MTP etched facet laser diode

The details of the laser coupon are in ***Table 4*** and an image of the laser is shown in ***Figure 13***.

Table 4. Standard Laser Coupon Information available for Europractice users

Standard Laser Coupon Information	
Material	InP
Thickness	Maximum 5.4μm
Laser threshold current	of the order of 20 mA
Maximum Power Output	of the order of 10 mW
Laser Geometry	
Metallization (Single Layer)	AU
Coupon Length	806μm
Coupon Width	86μm
Ridge waveguide width	2.5μm
Bondpad size (anode and cathode)	50μm x 50μm
Interpad separation	80μm in the x axis and 8μm in the Y axis
Centre of bondpad from coupon back end	152μm for the anode and 232μm for the cathode

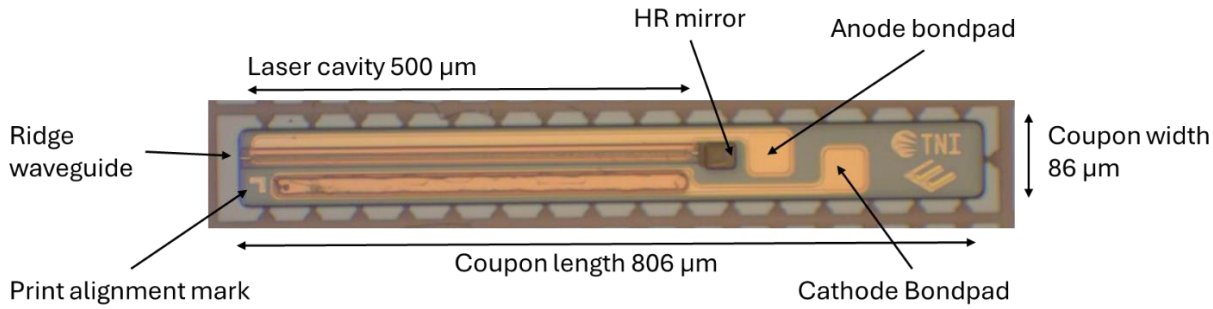

Figure 13. Representative image of the standard MTP laser offered in Europractice services

Laser diodes design rules

The design rules for the laser are as follows. The minimum print pitch for the lasers is 250μm on the Y axis and 856μm on the x axis. For array printing the minimum pitch is 250μm with an incremental increase of a multiple of 125μm in the Y axis and 856μm in the X axis (this reflects the source pitch). The laser waveguide offset from the centre of the coupon is 10.25μm and must be accommodated in any coupling structure. Currently, the maximum number of devices that can be picked and printed per array is 4. However, if a user requests an array printing more than this, a customized stamp have to be designed and procured. Please note that the cost of such a custom stamp is not covered of the service cost of the printing offered for Europractice users, and additional costs and service delivery time will be reflected to user.

In case users are interested to printing to non-Tyndall user substrates, a clearly visible preferably metallic alignment marker is essential with at least 15μm x 15μm in size, must be placed to left of the emitting facet within minimum of 75μm and maximum of 100μm in both the and X and Y axis relative to the centre of the laser coupon alignment marks. These marks cannot be obscured during the print cycle. When printing to a non-Tyndall user provided submount, the closest the laser coupon can be placed to a coupling structure is 1.5μm. The maximum surface roughness of the print area of any supplied target must not exceed 3nm. The devices are designed to be contacted by either wire bond connection of RDL. Wirebonding services can be provided by Tyndall but the maximum wire diameter than can be employed is 20μm due to bondpad size restrictions. We strongly recommend users carefully review and consider the design rules and contact Tyndall for technical review before fabrication of their devices, especially if the substrate is a PIC, in case they are interested in printing services for their substrates. Some general design rules for laser printing summarized in ***Table 5***.

Tyndall does not currently provide RDL services for printed lasers under Europractice but can be consulted and contracted to if this is chosen as an approach by the Europractice user. Please note that additional pricing and delivery time will be included for this, as this will be customised service.

Table 5. Design rules of lasers available for Europractice users

Laser Diode Design Rules	
Print Pitch	Y axis: >250μm **OR for arrays** 250μm with an incremental increase of a multiple of 125μm X axis: 856μm
Laser waveguide offset	10.25μm (accommodate for any coupling structure)
Alignment marks	Clearly visible - at least 15μm x 15μm
Alignment marks position	On left - 75μm (min) 100μm (max) in both X and Y axis relative to the centre of the laser coupon alignment marks
Surface roughness of print area	Not exceed 3nm
Wire diameter	20μm

Tyndall designed silicon submount for laser printing

The laser requires a target onto which it is printed. For Europractice users, Tyndall have fabricated Si based submounts for this purpose, and following are the details of this standard submount

The mount is fabricated for n-doped silicon with a 10 nm SiO_2 or AlN passivation layer on the surface to prevent electrical cross-talk between lasers and the laser contacts. Metal contacts are deposited onto the surface that act both as alignment marks for the µTP process and RDL lines onto which the lasers can be wirebonded. The RDL runs to contact at the edge of the submount for subsequent wirebonding to a PCB or probing. Prior to print of the laser the submount is coated in a thin polymer adhesion layer (50 nm of Intervia) to keep the devices in place during the wire bonding process. The submount is 5 × 5 mm in size with the laser print sites located at the centre of the left edge of the chip. The pitch of the laser print sites is exactly 250μm to facilitate coupling of the devices to a fibre array with a pitch of 250μm. The pitch of this cannot be adjusted due to constraints set by device size, printing pitch and fibre array pitch. Wirebonds are connected to RDL lines to the centre of the right-hand side of the submount to minimise wirebond length. The pitch between the contacts at the edge of the chip is 250μm. The top right-hand contact is a common cathode for the lasers and the other four address individual lasers.

A picture of the submount and lasers printed and wirebonded to the submount are shown in ***Figure 14***.

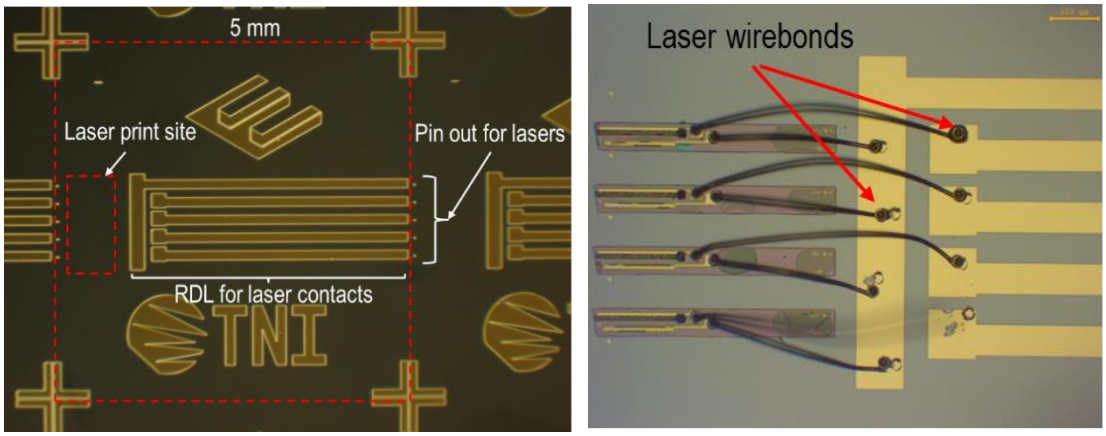

Figure 14. The MTP laser and the submount. Wide view of the submount prior to chip singulation (left), printed and wirebonded lasers on the submount (right).

Table 6 gives a summary of the standard Tyndall silicon submount.

Table 6. Details of Tyndall designed standard silicon submount available for Europractice users

Tyndall designed silicon submount	
Material	n-doped silicon with 10nm SiO_2 or AlN passivation layer
Metal contacts and RDL lines	Yes
Polymer adhesion layer	50 nm of Intervia
Dimensions	5 × 5 mm - the laser print sites located at the centre of the left edge of the chip
Laser print pitch	250μm
Pitch – contact and chip	250μm

Standard package for printed lasers

Tyndall provide different options for Europractice users depending on their needs, from only printing devices to submounts, wire-bonding, assembly to PCB, fiber attachment and to assembly in standard mechanical housing. Please note that these different options have different pricing and delivery depending on the required materials and services provided.

We have designed standard components – PCB, silicon submount, lasers, mechanical housing – and printing, optical and electrical packaging processes to provide low-cost packaging service for Europractice users. ***Figure 15*** and ***Figure 16*** represents design images and overall final package for laser printing with using Tyndall designed standard components.

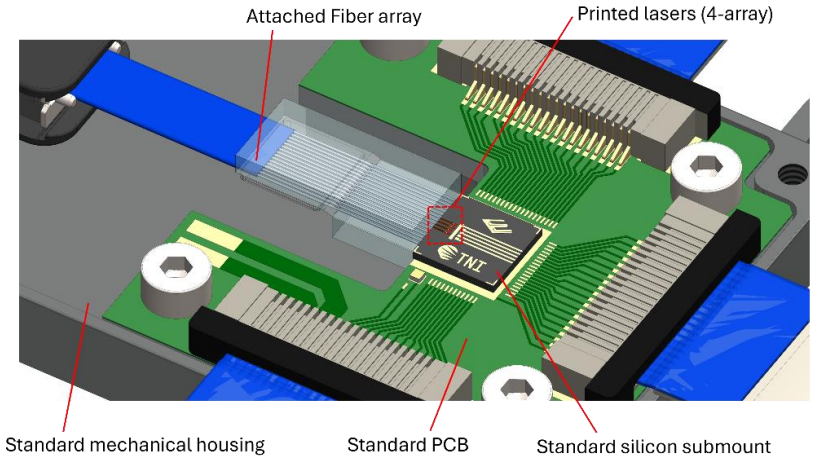

Figure 15. Overview of laser printing and packaging with Tyndall designed standard components

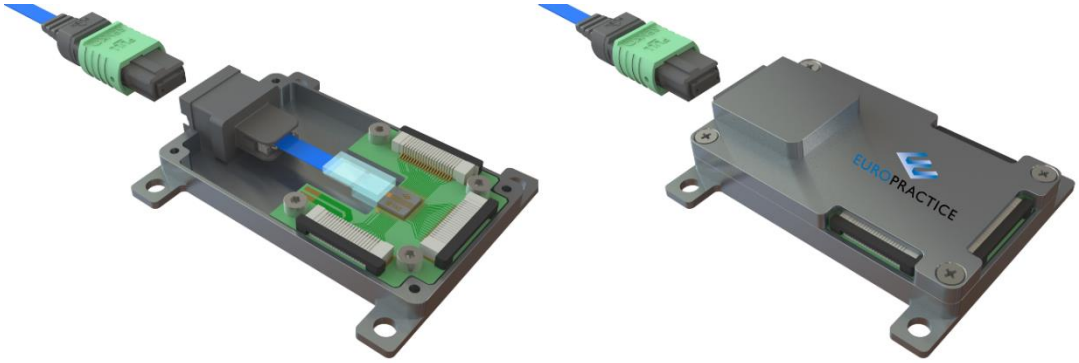

Figure 16. Overall package view offered for Europractice users, that includes all options for laser printing. Please note that the connector cable is not covered in our offers and given only for representative purposes.

Table 7 gives a summary of the initial offer for MTP laser diodes.

Table 7. Overall specifications of MTP laser diode package available for Europractice users

MTP package specifications (Laser printing)	
Tyndall Substrate material and dimensions	Silicon - 5mm × 5mm × 0.57mm
Maximum number of lasers	4
Laser pitch	250μm
DC connections	5
Optical Fibre connections	4 channels (Active)
Optical interface	Edge Coupling
Operating wavelength	1550 nm
Substrate	Si
RDL connection pitch	250μm
Mechanical housing dimensions	44.5mm × 54mm × 11.8mm

3.2.2. Uni-Travelling-Carrier (UTC) Photodiode Integration Service

For Europractice users, Tyndall designed a standard UTC PD and offers its printing onto either Tyndall submounts or substrates provided by those requesting the service. The UTC PD is InP based with a maximum thickness of 1.2μm including the laser epitaxy, dielectric coatings, and metal contacts. It can detect light of wavelengths ranging from 950 to 1550 nm. The maximum frequency at which this device can operate has been measured as 90 GHz. This speed has been measured though probe testing, therefore please note that a fully packaged device in this offer will not give this performance as specialised interposers and connections would be required. Specialised RDL lines are required to drive these devices as bondpads are too small to accommodate wirebonding. An image and schematic of the photodiode is shown in ***Figure 17***.

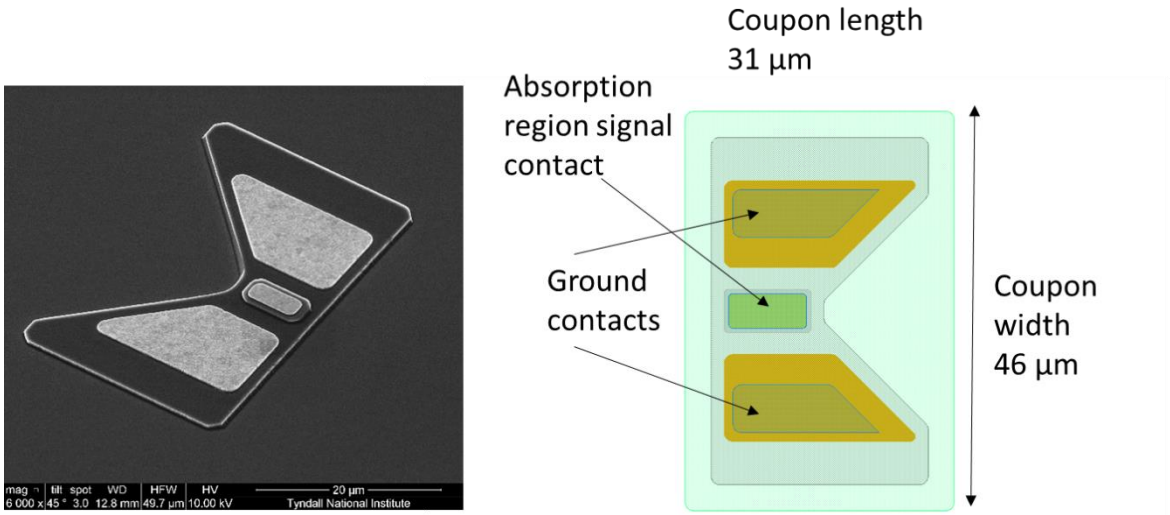

Figure 17. Transfer printed UTC PDs on Silicon. SEM image of a printed UTC PD (left), Schematic of the UTC PD (right).

UTC Photodiodes design rules

The design rules for the photodiode are as follows. The coupon is 31μm long and 46μm wide. The minimum print pitch for the photodiodes is 84μm on the Y axis and 100μm on the x-axis. The photodiode absorption region is located at the centre of the Y axis of the coupon at starts 4.5μm from the front of the coupon and is 10μm in length. The coupling to the absorption region of the photodiode is evanescent and a grating or other structure must be employed to couple for any waveguide. The absorption region at the centre of the coupon is 5μm × 10μm in side and the metal contact is 4μm × 9μm. The ground contacts are a maximum 10μm × 22μm and have a centre-to-centre separation of separation 11.5μm. For array printing the minimum

pitch is 84μm with an incremental increase of a multiple of 84μm in the Y axis and 100μm in the X axis (this reflects the source). When aligning to non-Tyndall substrates a clearly visible preferably metallic alignment marker at least 15μm × 15μm in size must be placed to left of the front on the coupon within minimum of 75μm and maximum of 100μm in both the and X and Y axis relative to the centre of the p-contact metal of the photodiode. These marks cannot be obscured during the print cycle. The maximum number of devices that can be picked and printed per array 48. However, if array printing is requested a specialised stamp will have to be procured. This cost of such a stamp is not covered by the service cost of the printing. The devices can only be contacted by RDL lines which need to be deposited after printing. On the supplied submount the pitch of the ground and signal contacts is 125μm with a width of 100μm. This will be discussed in more detail in the next section.

Table 8. Specifications of UTC photodiodes offered for Europractice users

Design Rules for UTC PDs	
Material	InP
Thickness	Maximum 1.2μm
Coupon size	Length (31μm) – width (46μm)
Detection range	950 to 1600 nm
Driving	RDL lines
Print pitch	84μm (Y axis) - 100μm (X axis)
Photodiode absorption region	At centre – starts from in front - length 10μm
Coupling to absorption region	Evanescent and grating
Absorption region	5μm × 10μm
Metal contacts	4μm × 9μm
Ground contacts	10μm × 22μm (maximum)
Pitch for array printing	84μm (minimum) with an incremental increase of a multiple of 84μm (Y axis) and 100μm (X axis)
No. of devices for array printing	4 (maximum)

Tyndall submount for UTC photodiodes

The photodiode requires a target onto which it is printed. For Europractice users, Tyndall Tyndall are fabricating SOI based submounts for this purpose. The mount is fabricated from SOI with a 220 nm device layer and a 2μm BOX layer. An 8 x 1 array of fibre grating coupling structures is formed for in coupling to SOI waveguides. The two outer couplers are for testing coupler and waveguide loss, the two inner ones adjacent to these are for aligning a fibre array and the four inner ones are for coupling to the photodiodes. The photodiodes are printed onto

a grating coupler which is connected to the fibre grating couplers via a silicon waveguide. SEM images of a test platform are shown in ***Figure 18***.

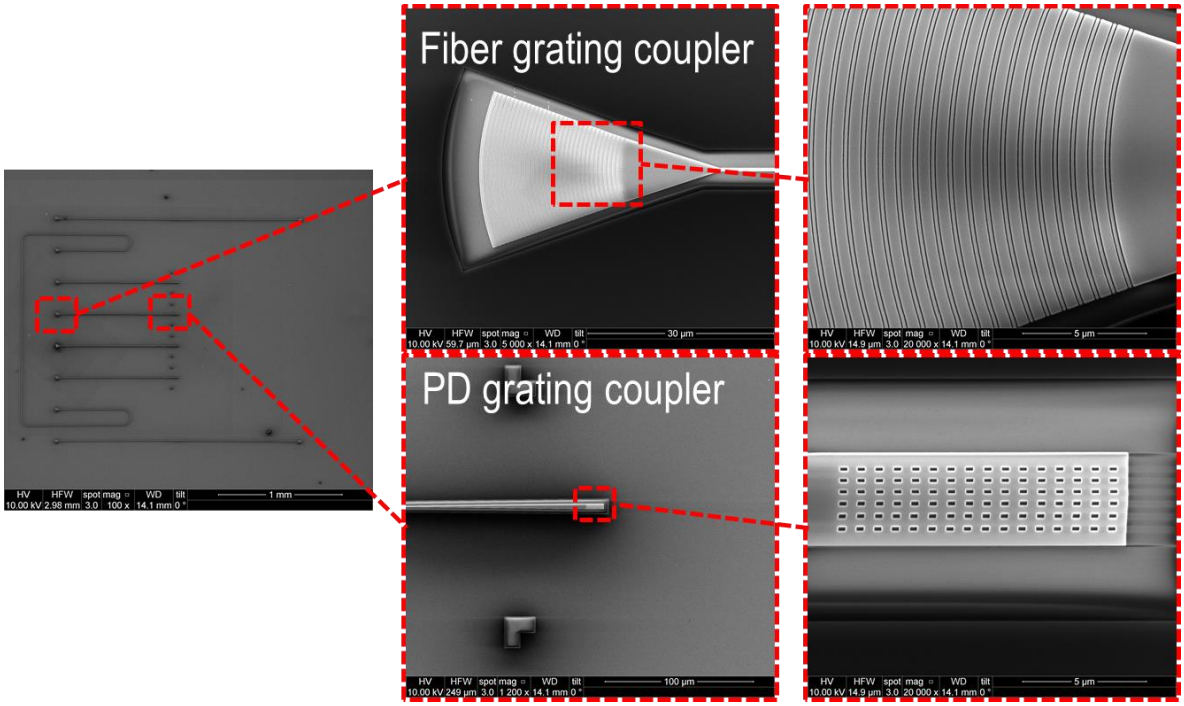

Figure 18. SEM images of the UTC photodiode transfer print target. (left) close up images of the fibre grating coupler and the photodiode grating coupler (right).

The photodiodes are printed to the PD grating couplers and then electrically connected via RDL lines that are deposited after the transfer print is completed. A schematic of this is shown in ***Figure 19***.

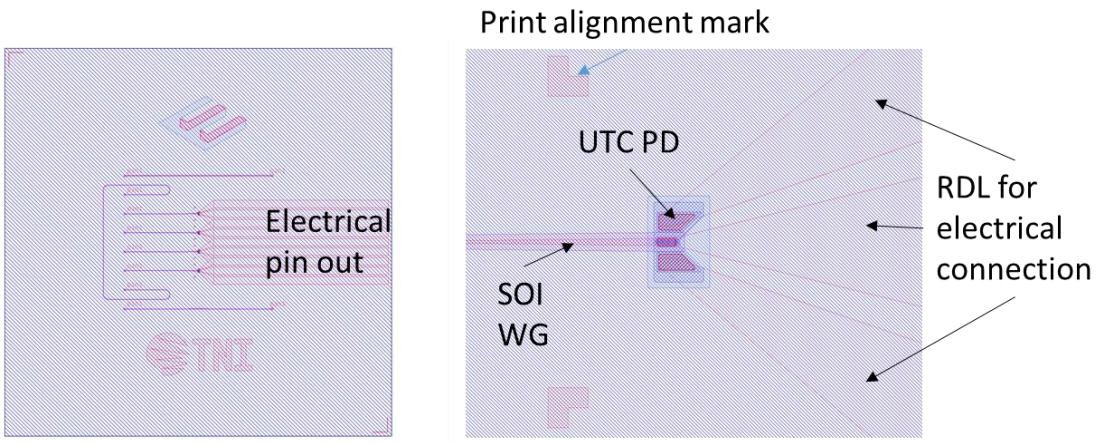

Figure 19. Schematic of the UTC photodiode (left) printed and wirebonded lasers on the submount (right).

The photodiodes are printed to the grating couplers and then electrically connected via RDL lines that are deposited after the transfer print is completed. A table of the specifications for the initial MTP UTC PD offer is shown in ***Table 9***.

Table 9. Specifications of UTC PD MTP offer

Design Rules for UTC PDs	
Submount dimensions	5mm × 5mm × 0.57 mm
Number of UTC PDs	4
UTC PD pitch	250 µm
DC connections	10
Fibre connections	8 (4 active inputs)
Fibre grating pitch	250 µm
Substrate	SOI
RDL connection pitch	125 µm

4. Europractice Chiplet Integration Service

Tyndall offers chiplet integration service of given standardized options at ***Section 3*** under a RUN-based service for Europractice users, which is called, Multi-Chiplet Run. Briefly, annual MPP-Run schedule will be announced in Europractice website and interested users should be reach out Tyndall by user interest form. During the technical evaluations between users and technical experts in Tyndall, user design is reviewed by Tyndall and once its compatibility to our offers is approved, users can proceed with pre-scheduled run registration in order to initiate service – see workflow at ***Figure 20***.

We strongly recommend to Europractice users interested in chiplet integration to review their designs with Tyndall before submission to a foundry, to avoid any issues at chiplet integration and packaging phase and to leverage of our services.

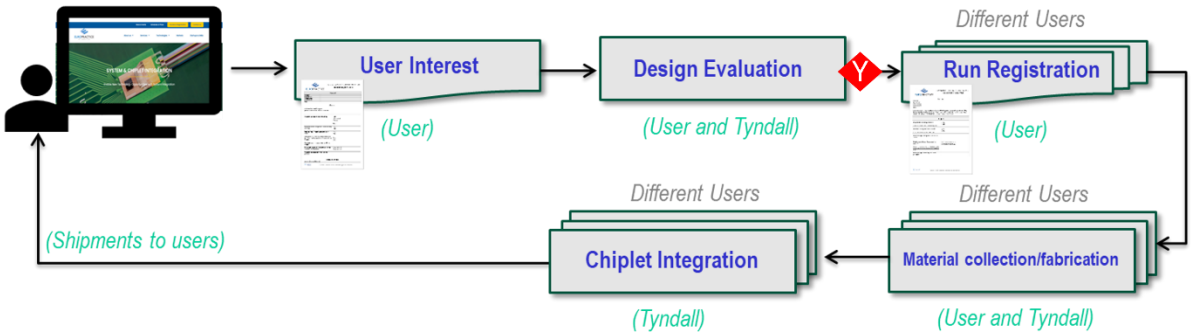

Figure 20. High level Chiplet-Run workflow. Please note that only users with approved design will benefit with offered standard packaging service.

This service is organized in order to reduce the integration and packaging cost-barrier to academic researchers and provide rapid turn-around time through standardized components and processes. We currently only offer the standard solutions provided in this document within Europractice, but we are continuing to develop our capabilities and grow the service, so check back soon for further updates to the packaging services we offer. Please note that our "Chiplet Integration Service" offers given in this document are different than those "Standard Packaging Services" offered by Tyndall, so interested users should refer to the "Packaging Design Rules".

5. Contact

This document is designed to anticipate the most frequently asked questions of MPW users wanting to access packaging and integration services. Both Tyndall and Europractice welcome user feedback that can be used to improve future versions.

Questions regarding technical solutions, pricing, delivery and packaging service RUN related should be addressed directly to Europractice (marc.rensing@tyndall.ie and ece.senel@tyndall.ie) who are part of the Photonics Packaging & System Integration Group at Tyndall, a Europractice partner.