ACTIVITY REPORT

2024-2025

EUROPRACTICE

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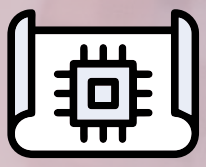
The access point for electronic circuits and systems for 30 years

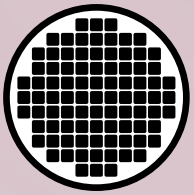
2024 at a glance

837 submitted designs



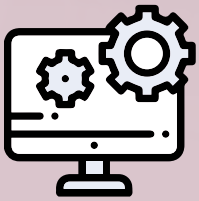
36 training courses

49 webinars on youtube



22 foundries in the technology portfolio

15 design tool vendors



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FOREWORD

Dear customers, colleagues and friends,

We are approaching a special milestone: Europractice will celebrate 30 years in 2025. This marks 30 years of successfully lowering the barrier to chip design and fabrication and faithfully serving our users by providing technical support and guidance. Looking back, we are proud to see how many cutting-edge projects our customers could accomplish relying on the services Europractice offers.

Today, we continue to support more than 600 European universities and research institutes and extend our support to early-stage startups, especially academic spinouts. In this report, alongside traditional user stories on prototyped designs, we invite you to discover exciting journeys of two ambitious startups that made their first steps together with Europractice, Deep Detection and NIT.

Continuing a positive trend, we observed a slight increase in the number of designs submitted for fabrication last year, reaching a total of 837. We are pleased to note that Europractice users are gradually transitioning to more advanced nodes, with the popularity of FD-SOI and FinFET technologies growing rapidly. Moreover, our technology portfolio has expanded and now includes fabrication services from 22 foundries, two of which, Graphenea and SINTEF, joined us last year.

In 2024, we continued to work on establishing a design IP exchange repository, providing system integration possibilities, and enhancing our training activities. We organized 36 in-depth training courses on design flows and different technologies, alongside 14 introductory webinars. For participants new to IC design, we hosted a comprehensive one-week-long Europractice Summer School that attracted 100 participants.

We are delighted that our efforts have been supported by Chips Joint Undertaking (Chips JU), enabling us to continue maintaining and extending the Europractice platform until September 2025. This year, we will work to secure a renewal of the EC funding which is essential to ensure that Europractice services can continue providing European academia and its spinouts with easy and affordable access to state-of-the-art design tools and IC technologies.

We express our gratitude to all of you – our academic and industrial customers, as well as our technology and design tool suppliers – for sharing this exciting journey with us.

Looking forward to supporting your innovative projects for another 30 years,
Your Europractice team at imec, UKRI-STFC, Fraunhofer IIS, CIME-P, and Tyndall

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EUROPRACTICE SERVICES

THE ACCESS POINT FOR ELECTRONIC CIRCUITS AND SYSTEMS

Europractice offers a platform with a full range of services to design and fabricate microelectronic circuits and systems. For 30 years, we have supported our customers in all critical steps from prototype design to volume production.

FABRICATION SERVICES

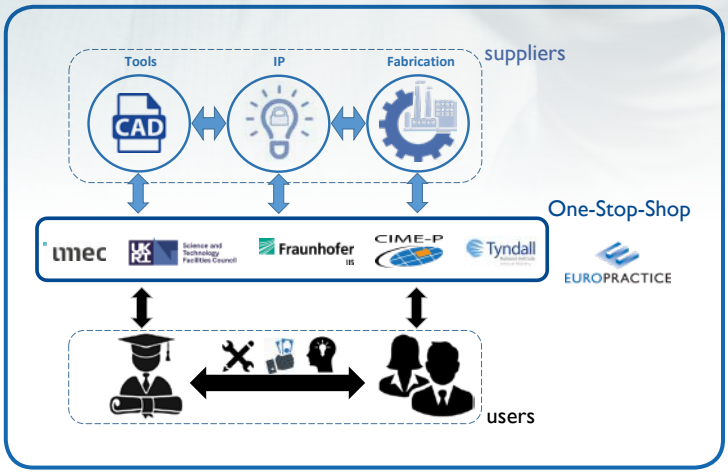
Cost-effective fabrication in technologies of leading foundries for both industrial and academic customers

DESIGN TOOLS

Affordable access to industry-standard design tools for European academia and its spinoffs

TRAINING & WEBINARS

In-depth hands-on training courses on design flows and technologies and free webinar series



Europractice acts as a one-stop shop representing the prime interface between the academic and industrial customers on the one hand, and the technology providers on the other. Our suppliers include design-tool and IP-library vendors, foundries, assembly and test houses – who all provide state-of-the-art industry-grade technologies.

Thanks to this coordinated brokerage service, the Europractice platform nurtures the growth of a microelectronic design ecosystem in Europe supporting industry and academia who look for affordable and easier access to electronic smart systems technologies. The barrier for users to access these technologies and services has been lowered by affordable pricing negotiated with vendors and, most importantly, by extensive customer support, stimulation and training.

As a result, Europractice has served as a pan-European chip infrastructure for design innovation, used by more than 600 European academic and research institutions and 300 European SMEs. The service builds on the many years of experience of five consortium partners: imec, UKRI-STFC, Fraunhofer IIS, CIME-P, and Tyndall.

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EXTENDING THE EUROPRACTICE PLATFORM

Celebrating 30 years in 2025, Europractice was launched with the support of the European Commission in 1995 as a successor to EUROCHIP (1989-1995) to enhance European industrial competitiveness in the global market.

Over the years, the platform has significantly evolved, continuously introducing new services and cutting-edge technologies, following the trends in the global industry.

In 2022 – 2025, Chips Joint Undertaking (Chips JU) has been supporting Europractice through a funded project RETICLES: Research, Entrepreneurship, Training, IP-exchange & Chip pLatform of Europractice Services. This project will nurture the further growth of the design ecosystem in Europe, building on the existing Europractice platform and further extending our offer. Here are some highlights:

RETICLES

DESIGN IP EXCHANGE REPOSITORY

Europractice is enhancing design efficiency through design reuse and establishing IP exchange repositories. Through these repositories, users will be able to share their IP and access the IP provided by other users. The first repository for exchanging microelectronic design IPs has already been established in collaboration with CERN.

SYSTEM INTEGRATION

The creation of smarter integrated systems has been stimulated through advanced system integration of dissimilar semiconductor technologies and chiplets.
In 2024 we expanded our System Integration portfolio by offering Micro Transfer Printing, a heterogenous integration technique where devices from one material system can be transferred from their native substrate material to a host substrate of a different material.

MORE SUPPORT FOR STARTUPS AND ACADEMIC SPINOUTS IN EUROPE

To support the semiconductor industry in Europe and create a breeding ground for deep-tech startups, Europractice provides a large scope of services to European SMEs:

- ✓ Prototyping in a wide range of technologies in multiple foundries.
- ✓ Route to upscale to volume production with a full package of required services, including test, characterization and qualification.
- ✓ Tailored training courses to meet the specific needs of individual companies.
- ✓ Affordable access to design tools for academic spinoffs.
- ✓ Support of the subsequent commercialisation of academic research.

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AFFORDABLE ACCESS TO STATE-OF-THE-ART CAD TOOLS

Europractice has negotiated lower prices with the major design tool vendors world-wide, as well as with IP and programmable device vendors. Consequently, European academic institutions can access Europractice licenses of the most advanced EDA/CAD tools for a wide range of electronic system (including IC, MEMS, Photonics etc.) design at affordable prices for education and non-commercial research. The design tools are made available in vendor specific functional bundles that are cost effective, easy to install and are enhanced annually under maintenance contracts to add new functionality. In addition, the Europractice service provides an infrastructure to allow its Members to access EDA/CAD vendor material, such as training material, on a scale which otherwise would not be possible.

The current Europractice network of European academic institutions is the largest network in the world having a unique and uniform tool base for electronic system, IC, MEMS and Photonics design. Access to these advanced CAD tools allows our customers to participate in EC-funded projects, ranging from IP block and component design to the design of complete systems.

altera An Intel Company · AMD · arm · cadence · COVENTOR A Lam Research Company · DESIGN WORKSHOP TECHNOLOGIES · HDL Works · IntelliSense · LUCEDA PHOTONICS · MZ TECHNOLOGIES · SIEMENS · SKILL CAD Accelerating Custom IC Layout · softMEMS · SYNOPSYS · XJ TAG

DESIGN TOOLS FOR ACADEMIC SPINOFFS

Spinoffs of European universities can access certain design tools at low cost via Europractice in order to produce a proof-of-concept IC to demonstrate their IP/product. The resultant IP can then be fully commercialized for an additional agreed fee. The spinoff gains access to an industry-standard full IC design flow, suitable for all IC technologies.

Europractice works flexibly with academic institutes and SMEs to facilitate effective innovation. For instance, we have mechanisms in place if an academic institute has developed a design using Europractice tools and subsequently wishes to exploit this design commercially, either via a spinout or by transferring the IP to an existing SME.

EASY ACCESS TO PROTOTYPING

It is challenging for small companies, academic and research institutions to obtain access to foundry fabrication lines since they often need a high level of technical support and require only a small-volume production for prototyping purposes. If they choose to work directly with a commercial foundry, the manufacturing costs will be very high.

This is when Europractice comes into play. We help significantly reduce fabrication costs by opening access to Multi-Project-Wafer (MPW) runs and Multi-Level-Mask (MLM) services for prototyping and volume production respectively.

In addition, Europractice offers a wide choice of technologies of world-leading foundries together with technical support and training.

TECHNOLOGY PORTFOLIO

The Europractice portfolio includes a broad range of technologies, such as ASIC processes ranging from 0.35µm to 7nm, MEMS, Silicon and Glass Photonics, Compound Semiconductors, Microfluidics, Flexible electronics and more.

New technologies and foundries

In 2024, the Europractice portfolio was further extended and included fabrication services of two more foundries. Our users can now access PiezoMEMS technologies of SINTEF and Graphene process flows of Graphenea. We also began offering the imec N2 Pathfinding PDK (P-PDK) for virtual designs developed within the NanoIC pilot line.

Traditionally, Europractice focuses on technologies from European-based companies as 19 of the 22 foundries have manufacturing facilities in Europe.

MULTI PROJECT WAFER AND MINI@SIC RUNS

By combining several designs from different customers onto the same mask set of a prototype run, known as Multi-Project-Wafer (MPW) run, the high cost of the mask set and the fabrication process is shared among the participating customers.

Fabrication of prototypes can therefore be as low as 5% to 10% of the cost of a wafer run for only one dedicated customer. A limited number of IC prototypes, typically 20-50, are delivered to the customer for evaluation, either as naked dies or as encapsulated devices. Only prototypes from fully qualified wafers are taken to ensure that the chips delivered will function "right first time". To achieve this, extensive Design Rule and Electrical Rule Checkings are performed on all designs submitted to the Service.

Since most of the designs fabricated for educational purposes are much smaller than the minimum block size on regular MPW runs, the concept of **mini@sic** was introduced in 2003. This solution allows to further lower prototype fabrication costs compared to standard MPW runs. The mini@sic principle is based on the following methodology: Several times per year, a foundry standard MPW block is bought and resold in smaller and cheaper sub-blocks or mini@sics. This program has been extended over the years and currently includes selected technologies from GlobalFoundries, IHP, TSMC, UMC and X-FAB.

TECHNOLOGY PORTFOLIO 2025

ams OSRAM

- ams OSRAM 0.35µm CMOS C35B4C3
- ams OSRAM 0.35µm CMOS C35OPTO
- ams OSRAM 0.35µm HV CMOS H35B4D3
- ams OSRAM 0.35µ HV CMOS OPTO
- ams OSRAM 0.18µm CMOS atC18C 0.8V/3.3V
- ams OSRAM 0.18µm CMOS atC18C 1.8/5V

em microelectronic

- EM 110nm CMOS ALP011 logic

GlobalFoundries

- GF SiGe 8XP
- GF 130nm BCDlite-Gen2
- GF 55nm BCDlite 55nm BCDlite
- GF 45nm SPCLO Si-Photonics
- GF 45RFSOI
- GF 45RFE
- GF 28nm SLPe
- GF 22nm FDSOI
- GF 12nm LP+

IHP

- IHP SG25H5_EPIC (BiCMOS + Photonics)
- IHP SG13S 0.13µm SiGe:C
- IHP SG13C 0.13µm SiGe:C
- IHP SG13G2 0.13µm SiGe:C
- IHP SG13G2Cu FEOL SG13G2 + Cu BEOL
- IHP SG13SCu FEOL SG13S + Cu BEOL
- IHP BEOL SG13
- IHP SG13S + MEMRES Module
- IHP SG13G3Cu 0.13µm SiGe:C
- IHP SG13G3 FEOL SG13G3Cu + Al BEOL
- Open-Source IHP SG13G2 SiGe:C
- Open-Source IHP SG13 CMOS

ST

- ST 28nm CMOSP28FDSOI
- ST 28nm CMOS28FDSOI
- ST 55nm BiCMOS055X
- ST 65nm CMOS065
- ST 130nm BiCMOS9MW
- ST 130nm HCMOS9A
- ST 130nm SOI H9SOI-FEM
- ST 0.16µm BCD8sP
- ST 0.16µm BCD8s-SOI

TSMC

- TSMC 0.13µm BCD+ (12")
- TSMC 0.13µm CMOS Log/MS/RF (G, LP)
- TSMC 90nm CMOS Log/MS/RF (G ,LP)
- TSMC 65nm CMOS Log/MS/RF (G, LP)
- TSMC 40nm CMOS Log/MS/RF (G, LP)
- TSMC 28nm CMOS Log/RF HPC/HPC+
- TSMC 22nm CMOS Log/RF ULL
- TSMC 16nm CMOS Log/RF FinFET Compact
- TSMC 7nm CMOS Log/ RF FinFET

UMC

- UMC L180 Logic GII, MM/RF
- UMC L110AE Log/MM/RF
- UMC L65N Log/MM/RF (LL)
- UMC 40N Log/MM – LP
- UMC 28N Log/MM – HPC

xfab

- X-FAB XH035 0.35µm HV
- X-FAB XH035 Noble Metal
- X-FAB XH018 0.18µm HV NVM E-Flash
- X-FAB XT018 0.18µm HV SOI
- X-FAB XS018 0.18µm OPTO
- X-FAB XP018 0.18 µm NVM
- X-FAB XR013 0.13µm RF SOI/XIPD
- X-FAB XT011 0.11µm HV SOI
- X-FAB XMB10 MEMS

AMF

- AMF Si-Photonics

CEA-leti

- CEA-leti Si-Photonics Si-310
- CEA-Leti SiN-Photonics Si_3N_4-800
- CEA-Leti MAD200 130nm NVM

CORNERSTONE

- CN Si-Photonics 220 passives/actives
- CN Si-Photonics 340 passives
- CN Si-Photonics 500 passives
- CN SiN-Photonics
- CN Suspended-Si
- CN Ge-on-Si

Fraunhofer

- 4H-SiC CMOS High Temperature Technology

Graphenea

- Graphenea PF1 – General
- Graphenea PF2 – Biosensing
- Graphenea PF3 – HKMG

imec

- imec GaN-IC on SOI 100V/ 650V
- imec Si-Photonics Passives+
- imec Si-Photonics iSiPP50G
- NanoIC imec N2 Pathfinding PDK

IMT

- Glass microfluidics

LIONIX INTERNATIONAL

- LNX SiN-Photonics TriPleX VIS
- LNX SiN-Photonics TriPleX 550
- LNX SiN-Photonics TriPleX 850

Pragmatic

- Pragmatic FlexIC Platform Gen 3

Science

- Science MEMS PolyMUMPS
- Science MEMS SOIMUMPS
- Science MEMS PiezoMUMPS

SINTEF

- SINTEF Thin-Film PiezoMEMS

teem PHOTONICS

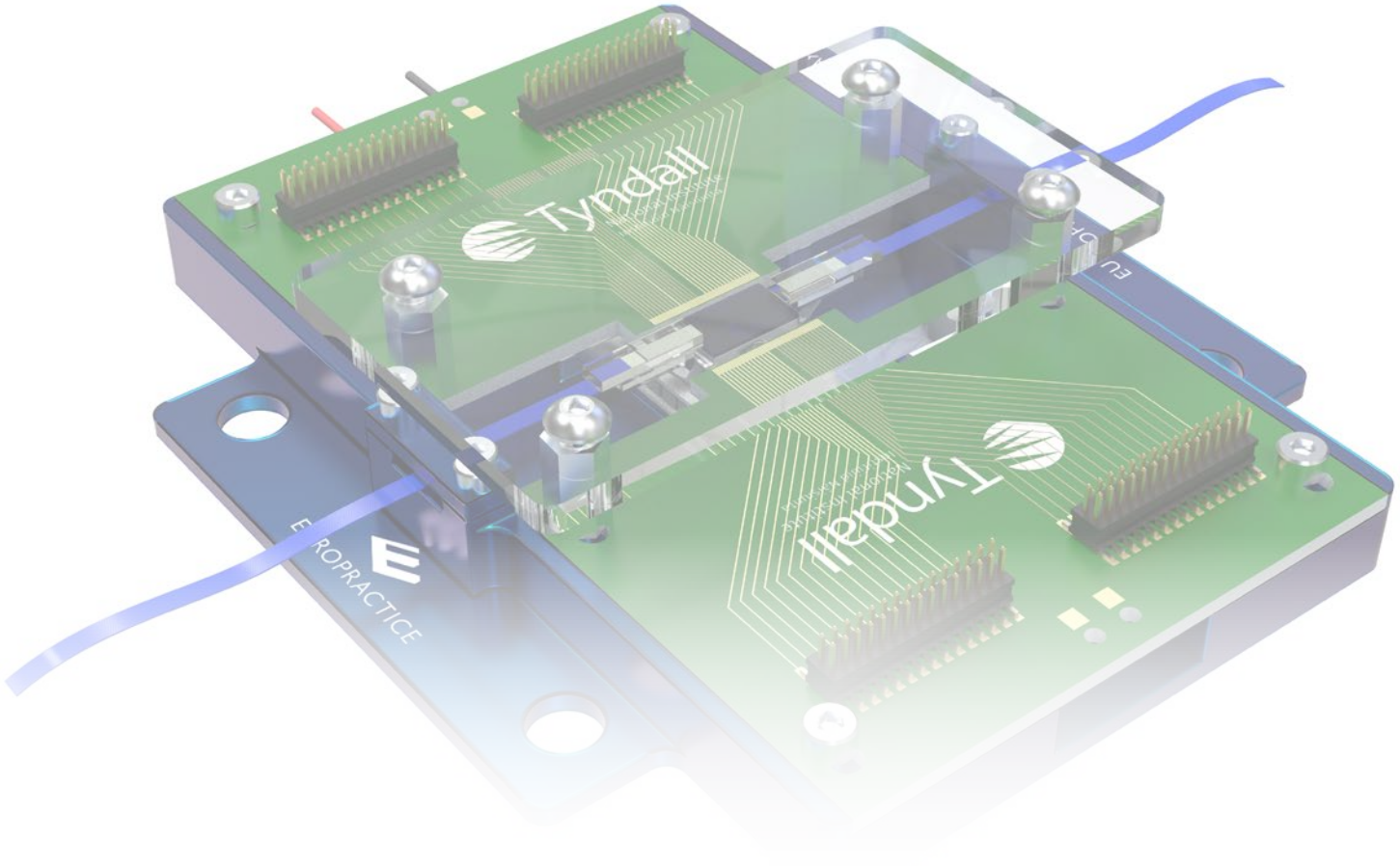
- Glass-Photonics IC ioNext-NIR
- Glass-Photonics IC ioNext-VIS
- Glass-Photonics IC WAFT

Tyndall National Institute

- PiezoMEMS Single electrode layer stack
- PiezoMEMS Dual electrode layer stack

United Monolithic

- UMS GH25 0.25µm GaN HEMT
- UMS GH15 0.15µm GaN HEMT
- UMS PH10 GaAs pHEMT



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MULTI-LEVEL MASK SINGLE USER RUNS

Another technique to reduce the high mask costs is called Multi-Level Mask (MLM). With this technique the available mask area (for example 20mm × 20mm field for stepper equipment) is typically divided in four quadrants (4L/R : four layers per reticle) whereby each quadrant is filled with one design layer. As an example: one mask can contain four layers such as nwell, poly, ndiff and active. The total number of masks is therefore reduced by a factor of four. By adapting the lithographical procedure, it is possible to use one mask four times for the different layers by using the appropriate quadrants. This technique allows to significantly decrease the mask costs.

The advantages of using MLM single user runs are:

- lower mask costs
- an MLM run is organized for one customer
- it can be scheduled for any date since it does not depend on regular MPW runs
- a customer receives a few wafers, resulting in a few hundreds of prototypes

The MLM technique is preferred over MPW runs when the chip area becomes large and when the customer would like to get a higher number of prototypes. When the prototypes are successful, this mask set can be used under certain conditions for low-volume production.

MLM runs are available for technologies from IHP and X-FAB.

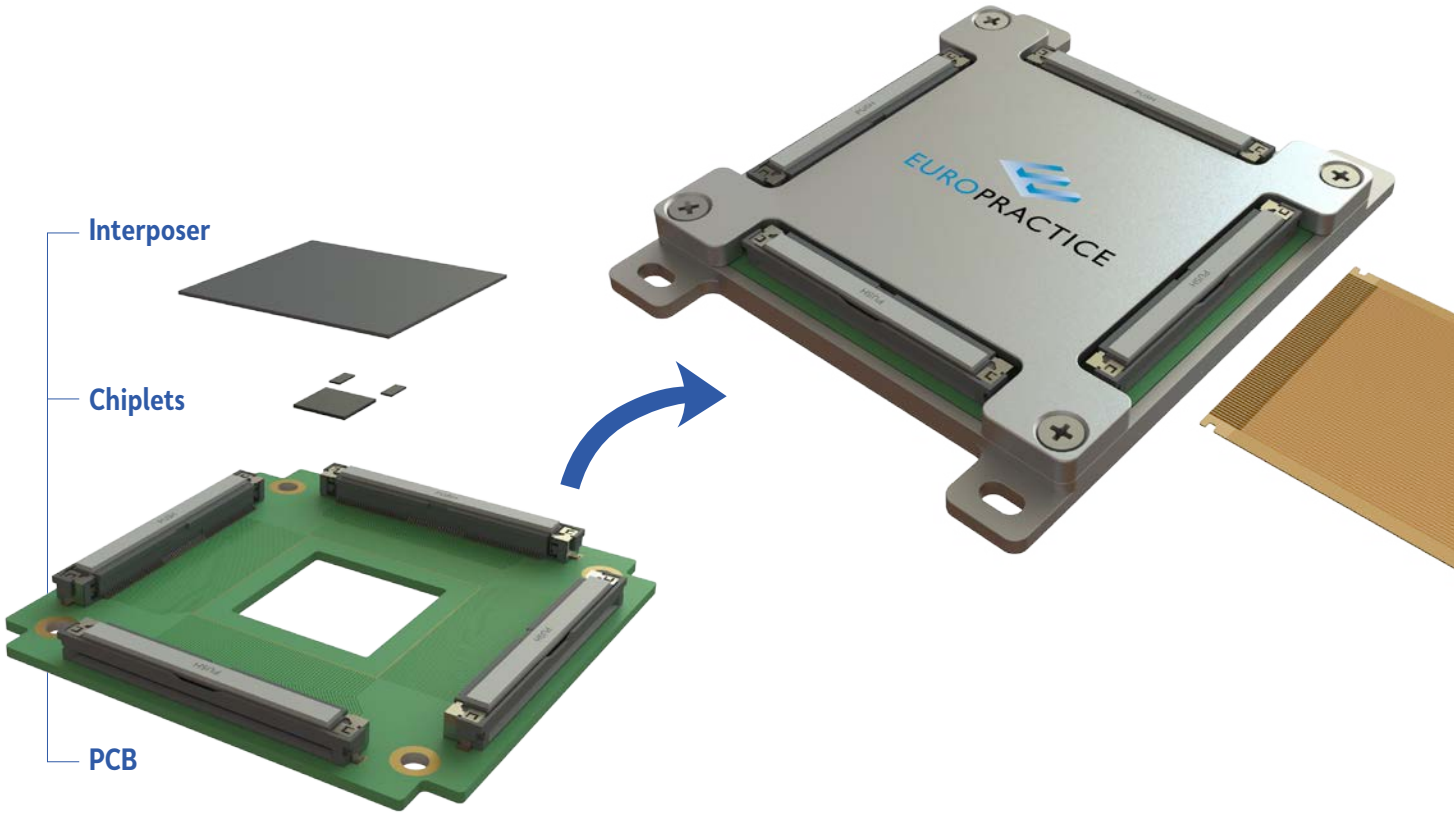
PACKAGING

Standardly, Europractice delivers unpackaged untested prototypes. However, Europractice offers a low-cost, flexible and coordinated packaging service using industrial qualified packaging houses. A wide variety of ceramic and plastic packages are available, ranging from DILs (Dual-in-line) to PGAs (Pin Grid Array) and QFNs (Quad-Flat No-leads). Alongside standard options, Europractice offers customized solutions and supply chain management to meet specific needs.

MULTI-PROJECT PACKAGING

In 2024, Europractice introduced Multi-Project Packaging (MPP) services for Photonic Integrated Cisrcuits (PICs). Similar to MPW runs, our new MPP service follows a scheduled approach to the PIC packaging . It is based on standard photonic package designs and processes and supports the packaging of PICs which require fiber coupling via grating couplers, edge couplers or single lensed fibers.

As the new MPP service is based on standardised packages and scalable processes, it helps to lower the cost barriers of packaging PICs and reduces turn-around times, while also allowing for a route to volume production.



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Single layer silicon interposer from Tyndall National Institute.

SYSTEM INTEGRATION

There is a growing demand for advanced packaging and system integration in the semiconductor industry. This trend has been fuelled by the need of a wide range of applications for better integration of more functionalities in a system-on-chip (SoC) and system-in-package (SiP).

Currently, the Europractice portfolio is being extended with advanced packaging and system integration services enabling customers to realise complex multi-technology devices that can be upscaled from early-stage prototypes to volume manufacturing. Europractice provides access to a variety of specialized process modules, including 2.5/3D integration of ASICs and PICs through die stacking techniques using pick-and-place, flip-chip, BGAs, Cu pillars, wafer-level fan-out packaging, as well as silicon interposers.

In 2024 we have expanded our System Integration portfolio by offering **Micro Transfer Printing (MTP)**, a heterogenous integration technique where devices from one material system can be transferred from their native substrate material to a host substrate of a different material. MTP can be carried out at the single die-to-die level or at wafer level for multi-chip transfer and lends itself to scaling to volume production levels.

Our new optical **chiplet integration offer** includes etched-facet InP lasers and high-speed photodiodes printed onto silicon substrates. A standard silicon submount is available for evaluating these new transfer printable lasers or users may supply their own compatible platform for printing.

Interposers play a vital role in chiplet-based architectures by providing high-performance interconnections between multiple chiplets, facilitating efficient communication and seamless integration. To support the adoption of chiplet-based designs among academic institutions and SMEs, Europractice offers interposer technologies spanning various levels of technology integration from different manufacturers, such as TSMC, ams OSRAM, and IHP.

Moreover, to allow users test their chiplet designs and encourage the adoption of chiplet based packaged modules, Tyndall offers the integration of electronic chiplets onto a standardised single layer silicon interposer, enabling 2.5D integration for DC applications. The service includes customised track routing, fabrication of single layer silicon interposers, flip-chip assembly, integration to a PCB and packaging into a low form factor package.

FROM PROTOTYPES TO VOLUME PRODUCTION

Once successful ASIC prototyping has been completed based on the MPW principle, we can also provide a clear route to volume production (from low to mid-high volumes). During this upscaling process, you work closely together with one of the Europractice partners, depending on the technology of your choice.

MIGRATION TO A FULL MASK SET

Based on a successful and validated prototype, the ASIC can be fabricated on a dedicated full mask set. One of the Europractice partners will take care of the production of the first engineering wafers and assist in the design and assembly of appropriate packages. Using their own bench tests, the designer can check the functionality of the ASIC produced on the full mask set.

DEVELOPMENT OF A TEST SOLUTION

When the device behaves according to the ASIC specifications, a test solution on an ATE (Automatic Test Equipment) platform is required to deliver electrical screened devices using a stable production test program. The test can be performed both on wafer level and on packaged devices. The goal is to screen the ASIC for manufacturing problems using the ATPG (Automatic Test Pattern Generation) and functional patterns. One of the Europractice partners supports you during the development of single-site test solution as well as with a multi-site test solution when high-volume testing is required. Any kind of volume production testing can be organised by the Europractice partners.

DEBUG AND CHARACTERIZATION

Before going into production, a characterization test program checks if all the ASIC specifications meet the customer's expectations. Threshold values are defined for each tested parameter. The software tests all the IP blocks and functionalities in the ASIC, and the results are validated against the bench test results. A characterization at Low (LT), Room (RT) and High (HT) temperature is performed on a number of (corner) samples together with statistical analysis (Cp and Cpk) to understand the sensitivity of the design against corner process variations.

QUALIFICATION

When the silicon is proven to be robust against process variations, the product qualification can start. Our partners can support you through the full qualification process using different kinds of qualification flows, including Automotive, Consumer, Industrial, Medical, Space, Military, Jedec and ESCC standards.
In this stage of the project, qualification boards must be developed for reliability tests and environmental tests.

YIELD IMPROVEMENT

Europractice partners can perform yield analysis to determine critical points during the production and suggest the correct solution to maximise the yield. During the characterization and qualification of the device on corner lots, the customer receives support in defining the final parameter windows. During the ramp-up phase, data of hundreds of wafers are analysed to check for yield incidents related to assembly and wafer production. The well-proven tool Examinator™ from Galaxy Semiconductor is used, enabling our engineers to perform fast data and yield analysis studies.

SUPPLY CHAIN MANAGEMENT

The responsible Europractice partner will manage the full supply chain for you. This highly responsive service takes care of the planning processes with the different actors in the value chain during both engineering and production phases. Integrated logistics ensures the accurate achievement of the final delivery dates.

PRODUCT ENGINEERING

Once the product is in steady production, the Europractice partner can assign a product engineering team to optimise the entire process for cost and efficiency. Insights from the initial production wafers may help, for instance, reduce test time.

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TRAINING IN DESIGN TOOLS AND TECHNOLOGIES

Europractice provides training courses targeting academic staff and PhD students from European universities and research institutes. Unlike training courses which address single topics or individual design tools, the Europractice training courses typically address a design flow which makes these training courses an efficient way to acquire new knowledge and ideally suited to new PhD students and junior engineers with a need to quickly become productive with a design flow.

Since the courses are based on the Europractice design tools, PDKs and Technologies, participants will be able to directly apply the techniques learnt on the training course when they return back to their own organization and make full use of the Europractice infrastructure in their innovation, research and training.

Courses include a strong element of practical sessions where participants have an opportunity to extensively practice the concepts described in lectures, and have access to experts who can answer questions about the concepts, design tools or technology processes discussed on the course.

Where a design flow is well supported by multiple vendors and/or processes, multiple course variants are offered that reflect the typical practice within European industry.

Over the last year, 36 courses provided training to 420 delegates, with 176 of these delegates being PhD students, many of whom will go on to become future industry and academic leaders.

A highlight of 2024 was the first edition of the Europractice Summer School. This was a comprehensive one-week-long training event that introduced participants into the world of IC design. We were delighted to welcome more than 100 participants who joined us at imec in Leuven, Belgium.

WEBINARS

To introduce the constantly growing service portfolio and share valuable technology insights, Europractice regularly develops and hosts highly successful webinars. These online events usually include informative presentations given by experts from world-leading companies, foundries or academic institutions, followed by a short Question & Answer session. All webinars are free of charge and open to a broad audience with different backgrounds.

In the past year, we hosted two webinar series that will soon be available on our YouTube channel:

Introduction to Photonic Packaging

This four-webinar series introduces key concepts essential to photonic package design, covering mechanical, thermal, electrical, and, most importantly, optical aspects. It focuses on the practical, engineering side of packaging, drawing on the extensive experience of the Tyndall National Institute.

Extending Webinar Series on Graphene

The webinar series on Graphene, co-organized by Europractice and the 2D Experimental Pilot Line (2D-EPL), has been extended with two new episodes covering the Graphenea process flow and the Graphene Photonic integration of IHP.

YouTube

49 videos with our recorded webinars are available on the official YouTube channel of Europractice Services, covering different technologies: Microfluidics, MEMS, Flexible Electronics, Graphene, Silicon-Photonics, advanced Photonics packaging and more.

Additionally, we organised a further four webinars on selected topics. These included a webinar on new Synopsys Simpleware tools and webinars on design techniques, such as applications of IJTAG, optimizing RISC-V for Application Specific Processor Design and Atomic-Scale Modelling of Complex semiconductor Materials.

Europractice webinars remain highly popular. Last year, the live-stream sessions were attended by over 100 delegates each.

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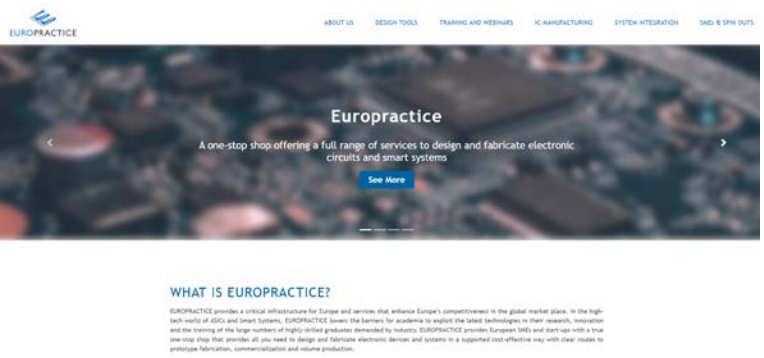
COMMUNICATION AND OUTREACH

At Europractice, we use a wide range of communication channels to increase awareness about our services and deliver the latest updates to both existing and potential users. Among online platforms, our web portal and social media channels play a primary role.

WEB PORTAL

The **General Portal** europractice.com is the main entry point for Europractice services, where you can find all the information you require.



For further details on one of the aspects of our portfolio, the portal will redirect you to:

- **Design Tool & Training website** europractice.stfc.ac.uk with the latest information related to Europractice membership, purchase of design tool licenses, upcoming training courses and webinars;
- **Technology & Fabrication website** europractice-ic.com with detailed information on the MPW offer, run schedules, and pricing.

SOCIAL MEDIA

We are happy to see that our Europractice community on LinkedIn and YouTube is growing. Following our accounts is a great way to stay informed about the latest service portfolio additions and share your experience with Europractice.

On **LinkedIn**, we do not just publish announcements of new technologies and services, but we also give visibility to our customers by publishing their testimonials and technical user stories. At the beginning of 2025, our LinkedIn community counted nearly 4.400 followers.

The **YouTube** channel Europractice Services gives a great opportunity to watch our webinar recordings. In February 2025, the channel had approximately 91.700 views and more than 1.83K subscribers.

LinkedIn announcement of our workshop at DATE 2024

CONFERENCES AND EXHIBITIONS

Every year, the Europractice team participates in various scientific conferences, industrial trade shows and fairs to present our services to existing customers and to attract new prospects.

In 2024, we were present at more than 20 events. For priority events, our consortium members delivered talks and staffed dedicated booths using promotional material designed in the well-recognisable bright-colour palette of Europractice.

We also continued organizing Europractice workshops at prominent European conferences. At DATE 2024, we hosted a workshop entitled "Tips and Tricks for a Successful Multi-Project-Wafer (MPW) Chip" to give a hand to less experienced MPW users. We are looking forward to presenting an improved version of it at ESSERC 2025 in Munich.

Europractice book display at ISSCC 2024

Europractice team at EFECS 2024

In 2025, we will attend at least the following conferences and fairs:

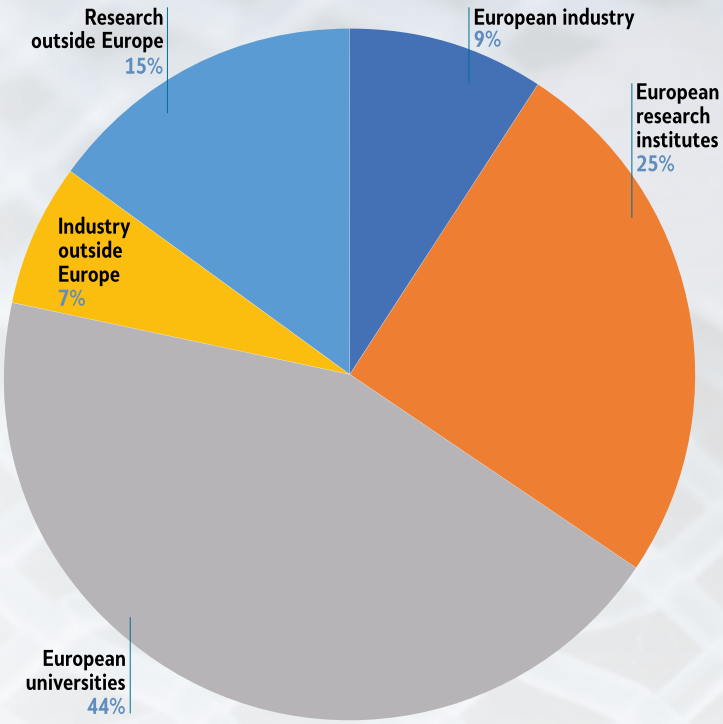
ISCAS 2025	London, UK	25-28 May
SMACD 2025	Istanbul, Türkiye	7-10 July
PRIME 2025	Taormina, Italy	21-24 September
ESSERC 2025	Munich, Germany	8-11 September
ISSCC 2026	San Fransisco, US	15-19 February

RESULTS 2024: MPW PROTOTYPING

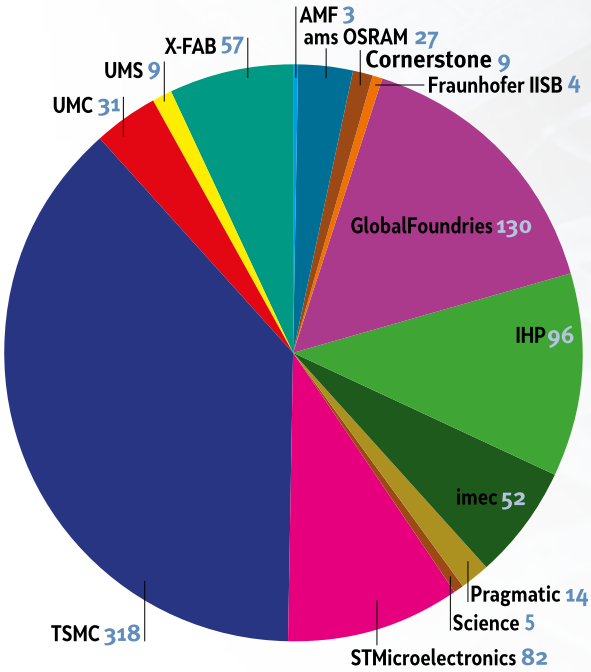
CONSISTENT AND STRONG DESIGN SUBMISSIONS

In 2024, the number of designs submitted for fabrication on Europractice MPW runs remained strong. Our users submitted a total of 837 designs for prototyping, marking a slight three-percent increase compared to the previous year. This consistent performance highlights that Europractice provides a reliable service that meets the diverse needs and requirements of our users.

As in previous years, the majority of designs (78%) were submitted by European users. Within Europe, universities and research institutes contributed 69% of the total submissions, while the industry, primarily SMEs and startups, accounted for 9%.



MPW designs in 2024



Number of fabricated designs in 2024 per foundry

ACCESS TO MULTIPLE FOUNDRIES

As in previous years, the majority of designs submitted in 2024 were manufactured by TSMC, a leading foundry in the global industry. The second place is occupied by another world-leading foundry, GlobalFoundries, whose numbers have grown by more than 40% over the past year. They were followed by the European R&D fab IHP and STMicroelectronics, one of Europe's leading foundries, which also showed significant growth in the number of submitted designs. Additionally, European foundries such as CORNERSTONE, Pragmatic, and UMS have seen notable increases in the number of prototyped designs.

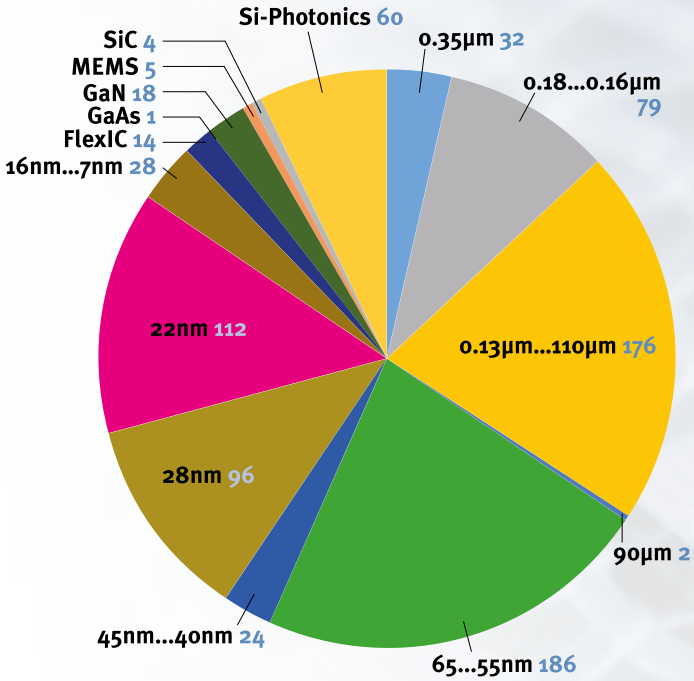
UNPARALLELED TECHNOLOGY MIX

Europractice lowers the barrier to access a very diverse range of technologies, encompassing advanced nodes, mature nodes, and More-than-Moore technologies.

We are pleased to see that Europractice users are gradually shifting to more advanced nodes. In 2024, the share of designs in mature technologies with nodes ranging from 0.11µm to 0.35µm decreased to represent one-third of all submissions, a decline of nearly 10%. Among the more advanced nodes, the 65nm technology and its associated nodes remain the most popular, with 186 prototypes fabricated.

Meanwhile, the number of designs in 22nm technologies has more than doubled, reaching 112, reflecting the growing popularity of both TSMC's 22nm ULL technology and, even more so, GF's 22FDX technology. Overall, FD-SOI technologies from GlobalFoundries (22nm) and STMicroelectronics (28nm) have shown significant growth, increasing from 72 designs in 2023 to 117 designs in 2024.

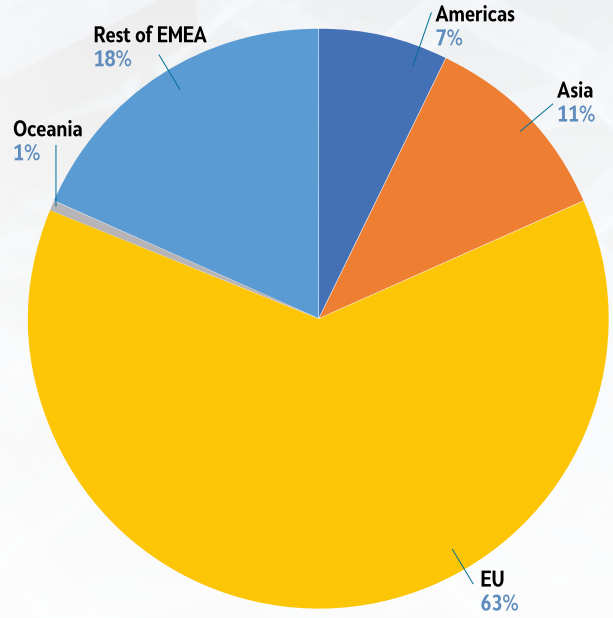
Additionally, the number of FinFET designs in TSMC and GlobalFoundries technologies has increased by one-third, reaching 28, mainly due to the rising popularity of the GF 12nm technology. Finally, the popularity of More-than-Moore technologies has also slightly increased, with a good uptake of the Flexible Electronics (FlexIC) offer from Pragmatic.



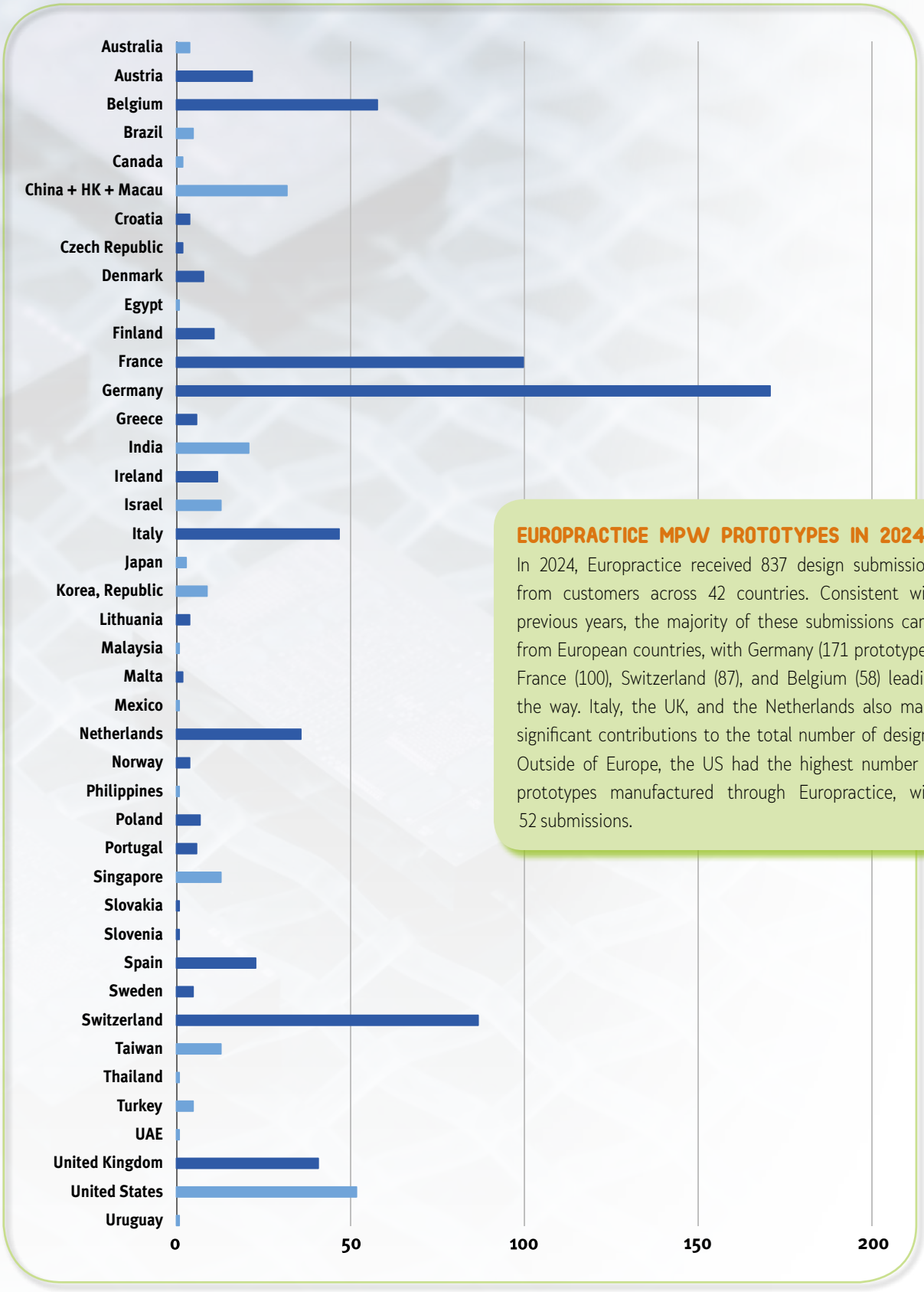
Number of fabricated designs in 2024 per technology (node)

EUROPE IN FOCUS

In line with previous years, over three-quarters of the designs fabricated in 2024 originated from Europe and the EMEA (Europe, Middle East and Africa) region, with the proportion of EU designs increasing to 63%. A moderate number of customers from Asia also used Europractice prototyping services in 2024. The remaining 8% of prototypes were manufactured for customers from the Americas (mainly the US) and Australia



Geographical distribution of MPW designs in 2024



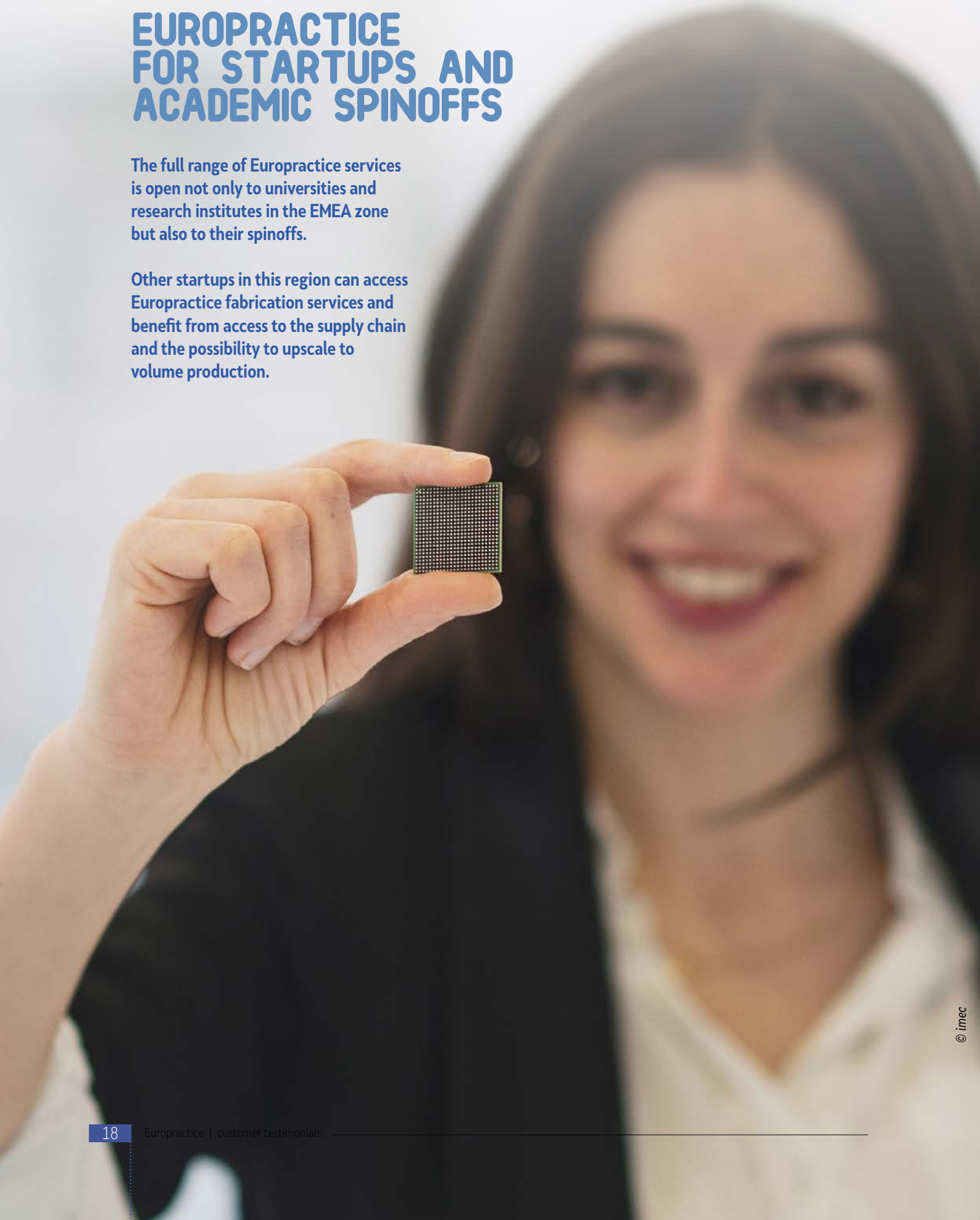
EUROPRACTICE MPW PROTOTYPES IN 2024

In 2024, Europractice received 837 design submissions from customers across 42 countries. Consistent with previous years, the majority of these submissions came from European countries, with Germany (171 prototypes), France (100), Switzerland (87), and Belgium (58) leading the way. Italy, the UK, and the Netherlands also made significant contributions to the total number of designs. Outside of Europe, the US had the highest number of prototypes manufactured through Europractice, with 52 submissions.

EUROPRACTICE FOR STARTUPS AND ACADEMIC SPINOFFS

The full range of Europractice services is open not only to universities and research institutes in the EMEA zone but also to their spinoffs.

Other startups in this region can access Europractice fabrication services and benefit from access to the supply chain and the possibility to upscale to volume production.



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Successful commercialisation of an academic design to transform on-line X-ray inspections

Deep Detection

Deep Detection is a spinoff from IFAE (Institut de Física d'Altes Energies), part of the Autonomous University of Barcelona (UAB). To help customers maintain the quality and safety of their products, Deep Detection has developed a new generation of X-ray cameras that go beyond the detection limits of conventional technology. How did they make their journey from an academic design to an industry-transforming product? What challenges did they encounter on the way? We discussed these questions with Colin Burnham, the co-founder and COO of Deep Detection.

Colin Burnham is the Co-Founder and Chief Operating Officer of Deep Detection S.L. which is dedicated to better inspection for a safer and more circular world. Prior to planning his transition into deep tech scale up he was an R&D head for European F&B and an executive board member. He developed a passion for bringing teams and technology together to create groundbreaking innovation in consumer products, nutrition, ingredients and advanced manufacturing for some of the world's favourite brands.

Colin holds a Chemistry BSc from the University of Birmingham and a Masters in UAV and Remote Sensing technologies from Universitat Politècnica de Catalunya.

Extending limits of industrial inspections

X-ray used in industrial inspections was black and white until Deep Detection introduced the benefits of colour using photon counting. Colin Burnham explains: *"X-rays carry information about the materials they pass through. The only way to unlock this information is to turn to photon counting. The detector directly measures X-rays and bins individual photons by their energy. This unlocks multi-energy or "colour" X-ray that allows us to improve inspection by detecting very small, high-risk foreign objects and lightweight contaminants, such as plastics. It is highly important for the Food and Beverage market, which we decided to focus on first."*

Today, the mission of Deep Detection is to bring photon-counting X-ray detectors to mainstream industrial inspection. In the meantime, their technology is also highly appreciated in other fields. For instance, Mayo Clinic – an American academic medical centre focused on research – commented: *"This type of advance in an imaging modality only comes along every couple of decades"*.

How did Deep Detection achieve these impressive results?

First steps from academic design to spinoff with the support of Europractice

It all began with a design created in IFAE. First prototypes were fabricated, packaged and tested using Multi-Project Wafer (MPW) services provided by Europractice.

Colin Burnham offers insights into the technology: *"The technology itself originated in particle detection. It was used, for instance, in High Energy Physics (HEP), galactic observation of X-ray and medical applications. Seeing an opportunity, researchers from IFAE chose to work on the ground-up design of a detector for industrial scanning. The focus has been to design a version of the technology suitable for industry, to make it affordable, robust, and effective in industrial scan applications."*

The Deep Detection team met through the Collider program of the Mobile World Capital accelerator, which helps create innovative technology start-ups by connecting scientific and entrepreneurial talents. To go to the next level and grow their enterprise, the team decided to participate in engineering runs with full wafers. This opportunity was also provided by Europractice.

"We were really happy with the support and guidance we received from Europractice, not only on chip fabrication but also on software and design tools. We opted for the Proof-of-Concept Cadence license, which Europractice makes available to academic spinoffs, in order to further develop our ASIC design and complete the first engineering runs. That allowed us to improve the functionality and stability of the research design to be industrially ready", elaborates Colin.

Fig.1: The PhotonAi® camera contains hybridised sensors for multi-channel photon counting during line scan inspection.

Launching new innovative products

Colin introduces PhotonAi® cameras that Deep Detection have designed to integrate into one product capabilities that are normally distributed across several cameras: *"All PhotonAi® cameras have as standard Pixel Precise dual energy, a key feature for unmasking foreign objects in complex products. Combining Pixel Precise material separation with smart analytics allows automated detection of foreign objects, even in complex products, like this test with pistachio nuts where you can see a lightweight glass fragment"* (see Figure 2).

"Our objective has always been to move from spinoff to scale-up with an industrial product portfolio. Throughout the journey, Europractice has been, and will continue to be, a key partner in enabling the design and manufacture of our core technology stack", concludes Colin.

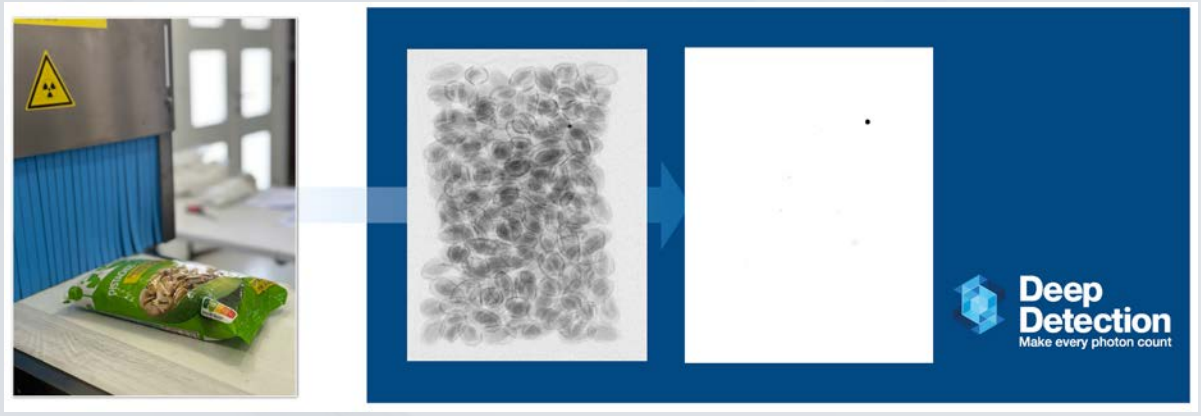


Fig.2: Product inspection test using Pixel Precise dual energy to automatically separate a light glass contaminant from pistachio nuts.

Successful collaboration between academia and industry advances infrared detector technology

New Infrared Technologies (NIT) is a Madrid-based Spanish company that develops and commercialises industrial cameras and solutions for real-time monitoring and smart control of laser-based industrial processes. These innovative solutions are powered by self-produced infrared cameras manufactured with unique technology. CEO Arturo Baldasano and CTO Germán Vergara shared insights into NIT's evolution from a young startup to a well-established SME, emphasising the pivotal role Europractice played in their journey.

Building an innovative infrared detector

Today, NIT manufactures uncooled Middle Wavelength Infrared (MWIR) detectors, cameras, systems and solutions, focusing on applications in industrial inspections and the automotive sector. Their innovative products are rooted in research that began over 20 years ago at the Spanish Ministry of Defence.

Germán explains: *"I used to work in the Ministry's research group, where we explored various technologies. One of them was the uncooled MWIR detector, which was unique at the time and had the potential to unlock new applications. There was no infrared image detector on the market that was completely uncooled in the wavelength range from 1 to 5 microns. This is why we decided to start a company to industrialise it, leading to the founding of NIT in 2009."*

Arturo elaborates: *"The initial technology was analog, but we decided to go fully digital to achieve higher resolution and better performance of infrared detectors. To transform an analog system into a digital one, we needed to design and fabricate a readout integrated circuit. However, as a young startup with limited funds and resources, accessing expensive design and fabrication services was a challenge. This is where Europractice helped us."*

Research collaboration enabled by Europractice

Europractice is well-known as a one-stop shop that significantly lowers the barriers to accessing design tools and fabrication services, primarily for academic institutions, research institutes, and their spinouts in the EMEA zone. But what about other startups not affiliated with academia? In addition to granting them access to prototyping services, Europractice facilitates their collaboration with academia, enabling IP/design transfer and subsequent commercialisation.

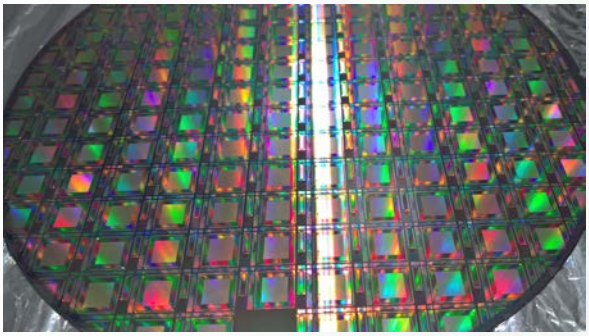
Germán shares: *"With the support of Europractice, the Institute of Microelectronics of Barcelona (IMB-CNM) was able to collaborate with us and handle the design of our chip. IMB-CNM provided expertise in readout integrated circuit development, while NIT contributed our know-how in infrared technology. This integration was crucial for creating a monolithic solution where the infrared*

Germán Vergara, PhD, is the co-founder and CTO of NIT. He earned his PhD in Physics from Universidad Autónoma de Madrid and served as a Visiting Scholar at the Electrical Engineering Department of Stanford University. With over 30 years of experience in basic science and applied technologies related to the study and manufacture of electro-optical devices, Germán has authored more than 60 scientific papers and holds 4 international patents.

Arturo Baldasano, MSc, MBA, is the co-founder and CEO of NIT. He holds a Master Executive degree from Instituto de Empresa de Madrid and is accredited as a Security and Features Authority by the London Stock Exchange. With over 25 years of experience, Arturo has held various managerial and directorial roles in the technology sector.

material is deposited directly on the CMOS, rather than using a hybrid approach. Together with IMB-CNM, we developed three generations of the readout integrated circuit, using first austriamicrosystems and then X-FAB technologies."

"We would not be where we are now without Europractice. It has significantly minimised risks, making it a perfect way to experiment and initiate new designs. Affordable fabrication services allow you to create new prototypes if you encounter problems and fix them. This continuous improvement is essential for successful development and growth, especially for young companies in the early stages", reflects CEO Arturo Baldasano on NIT's journey.



200 mm diameter Si-CMOS wafer with focal plane arrays sensitive in the MWIR spectral range monolithically integrated on it.

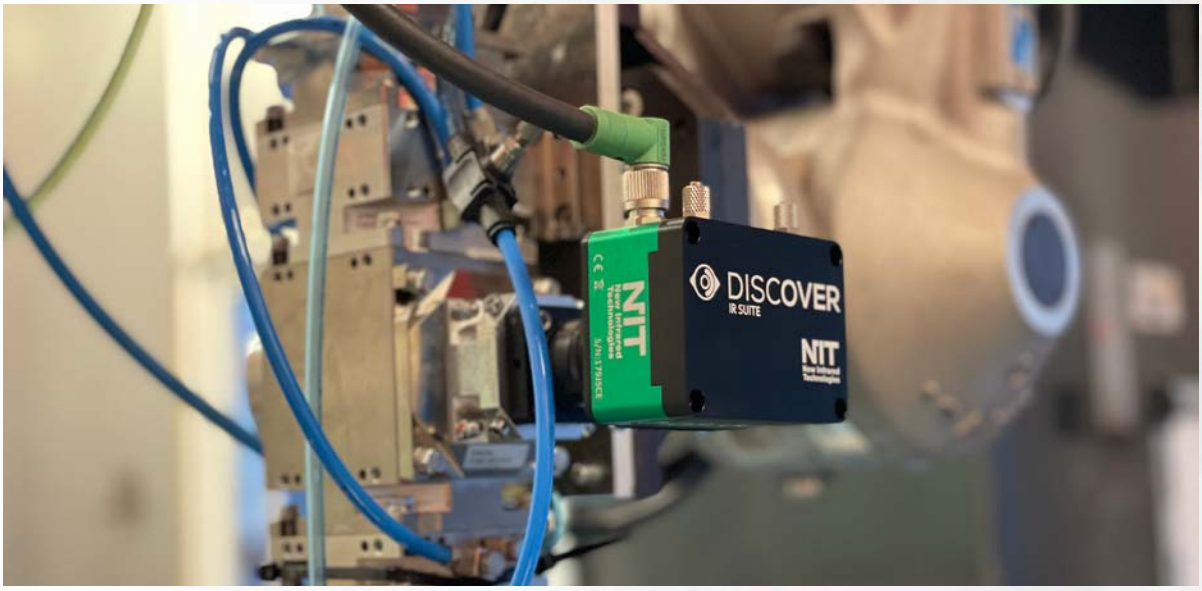
A successful partnership in infrared technology

The collaboration between New Infrared Technologies (NIT) and IMB-CNM has led to the successful development of unique, high-speed, fully digital infrared detectors now utilised in various industrial applications.

NIT's high-speed IR sensor, CLAMIR, attached to a laser head for monitoring and controlling industrial additive manufacturing processes in real time.

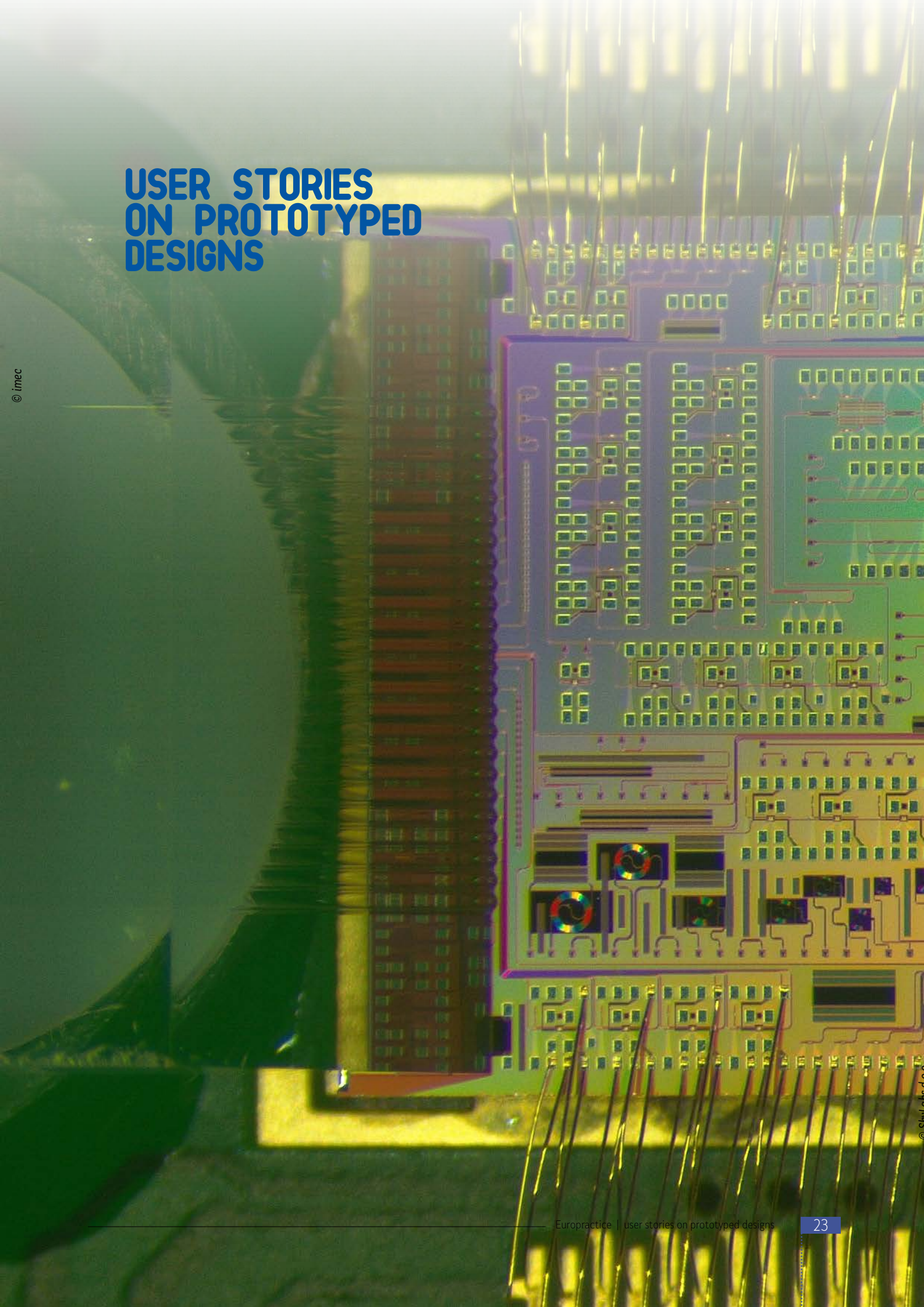
Germán elaborates: *"For instance, the technology is used for monitoring the laser metal deposition process, controlling it, and improving it in real-time to optimize process quality and energy efficiency. It is also applied in the automotive industry, specifically in reducing brake contamination, which is a significant contributor to vehicle emissions. NIT's system monitors the application of a thin layer on brakes to ensure compliance with upcoming Euro 7 standards."*

"NIT is currently a small company with a team of 10 people, focusing on leveraging collaborations and partnerships for non-core tasks. We are working on expanding our team and market presence, while increasing production capacity and continuing to invest in the development of new and improved infrared detectors. We are proud to say that we are now in discussions with a leading automobile manufacturer. Our success would not have been possible without the support of Europractice, and we highly recommend this platform to other startups", concludes Arturo.



NIT's high-speed IR sensor, DISCOVER IR SUITE, attached to a laser head for monitoring brake disc coating processes in real time.

USER STORIES ON PROTOTYPED DESIGNS



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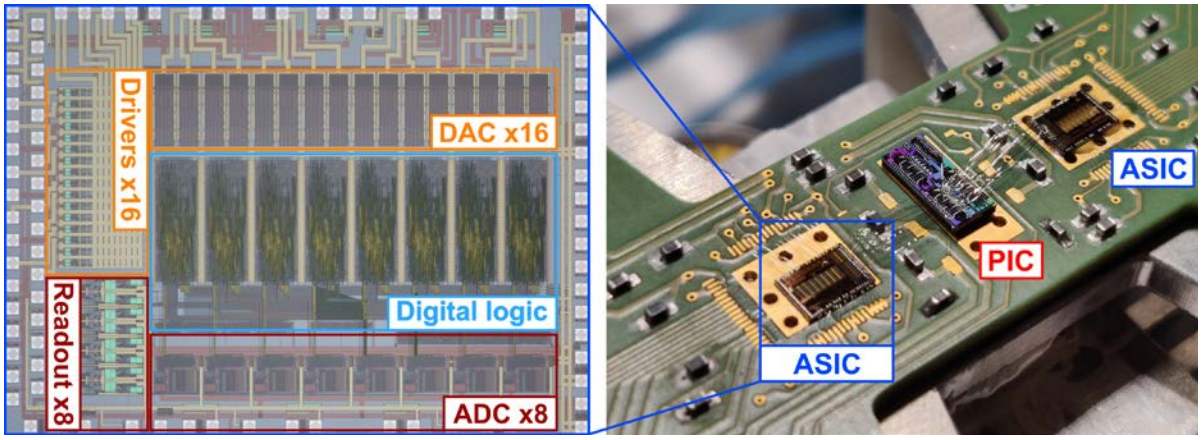

Fig.1: Chip micrograph and experimental setup.

Mixed-Signal CMOS controller for Integrated Photonic Processors

Department of Electronics, Information and Bio-engineering, Politecnico di Milano, Milano, Italy

Contacts:	Emanuele Sacchi, Francesco Zanetto, Marco Sampietro, Giorgio Ferrari
E-mail:	emanuele.sacchi@polimi.it
Technology:	ams OSRAM 0.35µm CMOS C35B4C3
Die Size:	4.1mm x 3.0mm
Design Tools:	Cadence: Virtuoso, Genus, Innovus
Application Area:	Datacom / Telecom

Introduction

Programmable photonic integrated circuits (PICs) can perform linear operations and signal processing directly in the optical domain[1]. Run-time reconfigurability is achieved through an electronic control layer that adjusts the working point of tunable elements, typically Mach-Zehnder Interferometers (MZIs), and stabilize them against drifts and perturbations of the input signal. As PICs grow in complexity (100-1000 interferometers) a scalable solution for the electronic controller is needed, one to be extended to large optical architectures whilst eating up only a fraction of power and area required by discrete-components designs. We thus designed an 8-channel ASIC that performs real-time configuration of complex PICs by addressing each component separately. Fig.1 shows how our electronics, that has a footprint similar to the optical processor, can be seamlessly replicated to achieve full control over a programmable PIC.

Description

Our ASIC closes a feedback loop around the PIC that senses and sets the working point of each optical element. In the case of a MZI, optical power is sampled on one of the two branches of the device; the measured signal is then filtered by an analog read-out scheme and digitized by a 10-bit SAR ADC, available in the technology libraries. The control algorithm, which relies on a lock-in modulation scheme[2], is implemented at digital level,

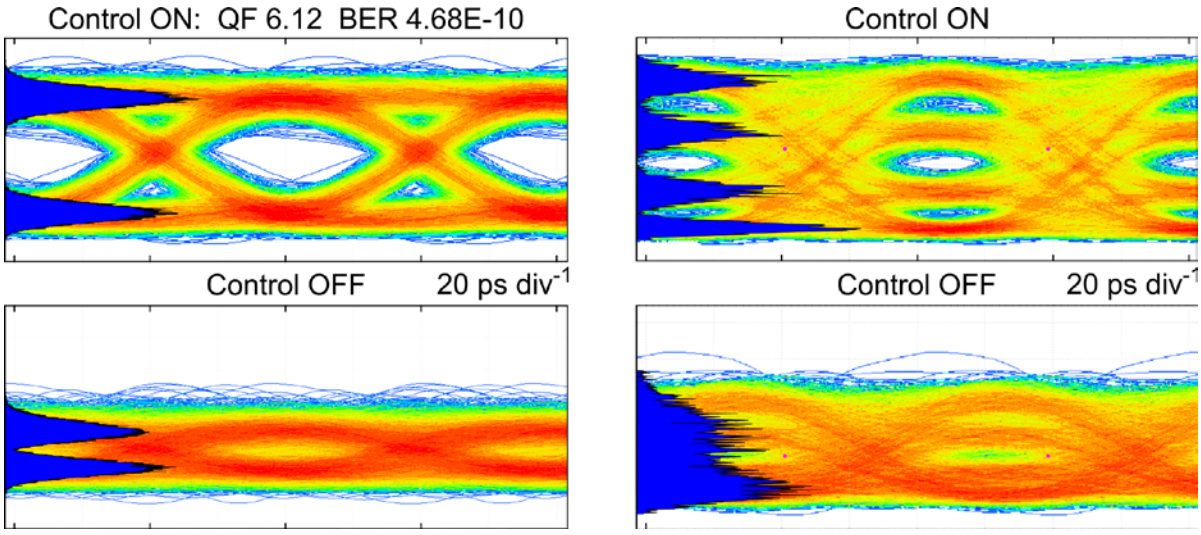

Fig.2: Measured eye diagrams at 25 (PAM2) and 50 (PAM4) Gbit/s.

ultimately defining the voltage applied to a pair of thermal actuators that regulate the phase shift in the branches of the MZI and hence determine the interference pattern at the output of the device. The digital circuit also features a serial interface to let the user define some parameters, mainly related to the bandwidth of the loop, which is estimated in 0.1-1 kHz. Overall, each ASIC consists of 8 channels which are totally independent, meaning that it is possible to let controllers work in parallel to operate complex programmable optical circuits.

Results

As shown in Fig.1, a pair of identical ASICs were wire-bonded to a 16x1 Silicon Photonics binary-tree matrix of MZIs used as a receiver in an free-space optical link [3]. Fig.2 illustrates the results obtained when transmitting PAM2/PAM4 signals at 25/50 Gbit/s, respectively: if the controllers are left off, the PIC cannot correctly receive the impinging free-space signal; instead, when the ASICs are active, each interferometer is driven independently in order to constantly match the configuration of the matrix with the ever-changing phases of the input wavefront, which may be altered by time-varying phenomena such as atmospheric turbulence. It is thus possible to reconstruct the signal directly in the optical domain, as demonstrated by the eye-diagrams measured at the very end of the tree of MZIs, with no need for additional high-speed DSP electronics.

Why Europractice?

Europractice offers to researchers an extensive technology portfolio and a rich calendar of general MPW and mini@sic runs. A comprehensive CAD suite and numerous seminars also ensure the designer is followed during every step of the process.

Acknowledgements

The Authors would like to acknowledge PoliFAB, the micro and nano fabrication facility of Politecnico di Milano, for wire-bonding the ASICs and mounting the experimental setup.

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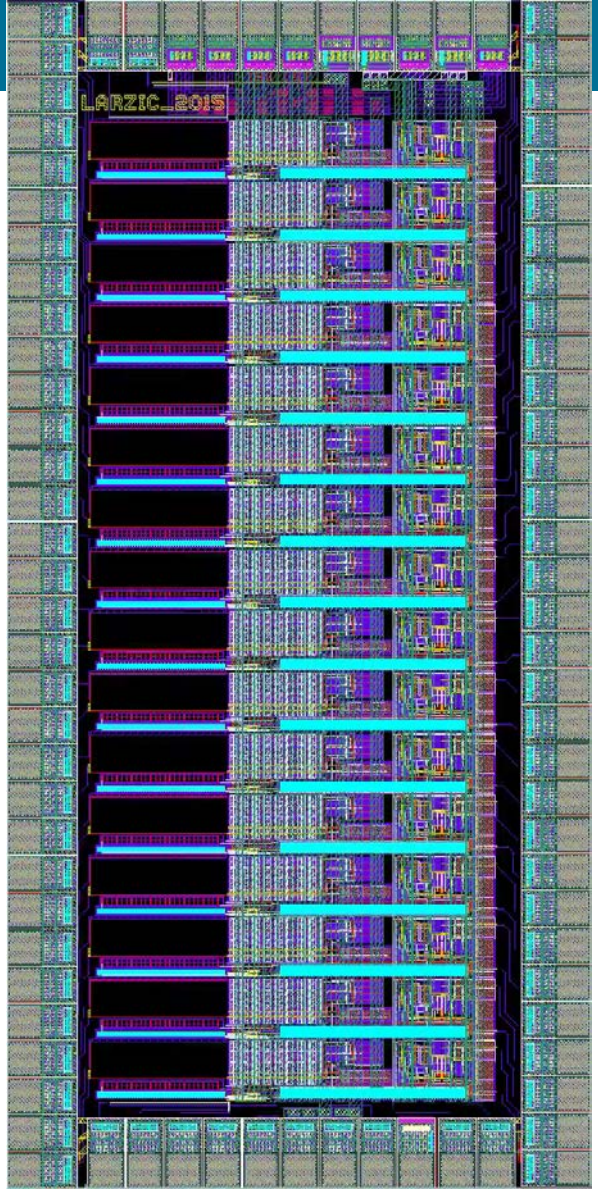

Fig.1: LARZIC 2015 layout.

LARZIC: Production of a Cryogenic ASIC for the DUNE experiment

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Technology: ams OSRAM 0.35µm CMOS C35B4C2
Die Size: 1657µm x 3368µm including pads
Design Tools: Cadence
Application Area: High Energy Physics (HEP)

Introduction

These LARZIC chips are used to equip the cryogenic analog Front End Boards (FEB) deployed to readout the top-drift Charge Readout Planes (CRP) of the Vertical Drift DUNE (Deep Underground Neutrino Experiment) Far Detector Module, containing a neutrino target made of 15kton of liquid argon. This detector is a huge liquid argon Time Projection Channel

Fig.2: LARZIC chip in a 100 pin PQFP 0.65mm pitch package for low-volume production in 2016, 2020, and 2023.

where the tiny ionization signals produced in liquid argon by charged particles, produced by neutrino interactions, need to be readout with low-noise cryogenic amplifiers and then continuously digitized with a total data bandwidth of 8 Tbit/s. The FEB operate just above the liquid argon surface at a temperature of about 110K.

The development of this cryogenic ASIC started in 2006, in view of its application in a future large liquid argon neutrino detector. Several prototyping steps were undertaken at IP2I, corresponding to different ASIC versions. The ASICs corresponding to the final version were exploited in many large-scale detector prototyping applications at the CERN Neutrino Platform (2015-2022), aimed at demonstrating the liquid argon detector technology for the DUNE experiment. More than 20,000 chips were eventually produced in 2023 in order to readout 256K electronic channels of the top-drift volume of DUNE Vertical Drift Far Detector.

Description

The LARZIC ASIC includes 16 readout channels. Each channel is composed by a Charge Sensitive Amplifier (CSA) followed by a differential output buffer stage, acting as low pass filter.

Peaking time	1 µs
Operation temperature	Typically around 110 K, the LARZIC/FEB can operate as well at LN2 temperature
Power consumption	11 mW/channel
ENC	≈ 600 electrons at cold for 250pF detector capacitance
Conversion factor	11 mV/fC (including all the entire analog chain ASIC + ADC buffer)
Calibration	Integrated charge injection system with embedded capacitors and the possibility of activating single channels or groups of channels
Integrated charge injection	1 pF
Unipolar dynamics (ASIC)	Linear up to 400 fC, max signals up to 1200fC with dual-slope regime (used in dual-phase)
Bipolar dynamics (ASIC)	Linear up to +-200 fC
Bipolar dynamics (ASIC coupled to ADC buffer)	Linear up to +-80 fC

The CSA has a linear gain for input charges of up to 400 fC and a logarithmic response in the 400–1200 fC range, corresponding to very high charge levels. This double-slope behaviour was developed to accommodate in principle stronger signals due to a high detector gain obtained by avalanche multiplication of the ionization in the gas phase (dual-phase liquid argon Time Projection Chamber), and of a single polarity due to the use of only collection views. This extended dynamics is not exploited in the Vertical Drift application where ionization signals in the detector are not multiplied in the gas phase. The double-slope behaviour is obtained by using a MOSCAP capacitor in the feedback network of the amplifier. The MOSCAP changes its capacitance above a certain signal threshold. Its capacitance value in the linear gain regime, of interest is 115fF, corresponding to a gconv value of 3.5 mV/fC. The MOSCAP then yields a lower gain for input charges larger than 400 fC, corresponding to a MOSCAP capacitance of 25 pF.

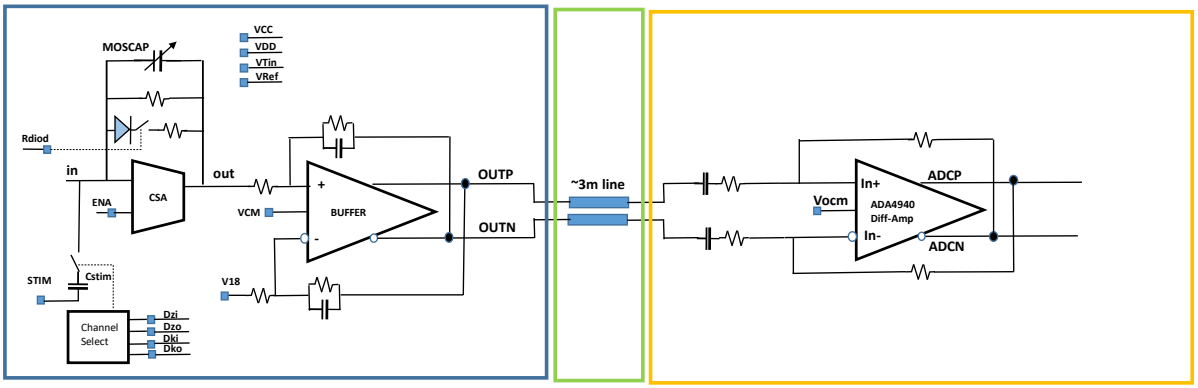

Fig.3: LARZIC ASIC cryogenic analog front-end with Charge Sensitive Amplifier and Buffer (left), Differential transmission line (middle), and AC coupled analog stage of the AMC (right).

Results

The ASIC amplifiers mounted on the FEB on the CERN large-scale detector prototypes have demonstrated to operate in a very reliable way (no channel failures) for many years with a noise lower than 1000 electrons. The channel-by channel response uniformity measured by including all the elements of the TDE analog chain is at the ~2% level. The results were reproducible in different detector tests operated at distance of time.

The ASICs were then massively produced in 2023 in order to instrument the readout of the top charge readout planes of the DUNE Vertical-Drift far detector module.

Why Europractice?

LARZIC chip has been developed since 2006 in several CMOS 0.35µm runs, using the CMP structure and MPW submission.

More recently, the large-scale production for the DUNE experiment has been managed in a dedicated 6 wafers run by CIME-P, a Europractice partner.
The Europractice service offers academic institutions and universities extremely useful opportunities for research in microelectronics at affordable prices.

Acknowledgements

This work was supported by CNRS-IN2P3, the LABEX LIO, IP2I and the MESRI DUNE IR* project

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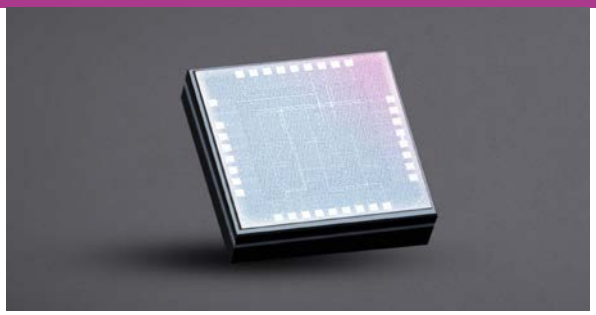

Fig.1: Layout of the high dynamic range and low power electrochemical analog front end testchip.

High dynamic range and low power electrochemical analog front end

CSEM, Zürich, Switzerland

Contacts: A.Sukumaran, F.Caruso, R.Cattenoz, B.Putter, J-L.Nagel, S.Emery and D.Manic
E-mail: amrith.sukumaran@csem.ch
Technology: GlobalFoundries 22nm FD-SOI 22FDX
Die Size: 1mm x 1mm
Design Tools: Cadence, Siemens
Application Area: Medical / Health

Introduction

The adoption of electrochemical sensing is gaining traction exponentially in a wide range of applications like continuous, real-time monitoring of chemical biomarkers through wearables, implantables and portable devices. Demand for rapid detection of pathogens and contaminants also drives adoption in agricultural and pharmaceutical applications.
We developed an ultra-low-power electrochemical sensing analog front end that can support various electrochemical measurements. It's a compact, ultra-low-power ASIC, implemented in GF 22nm that supports multiple electroanalytical methods (Chronoamperometry, various voltametric modes, and potentiometry). Since high dynamic range and low power are vital to accurately sense a wide range of analyte concentrations with minimal energy consumption, the focus was on optimizing these parameters which is absolutely necessary for portable applications.

Description

A compact and low power electrochemical analog front end that can support various electrochemical measurements has been developed. It's implemented in GlobalFoundries 22nm supporting amperometry, voltammetry and potentiometry. Its unique and proprietary biasing of the reference and working electrodes effectively enhances the sensor biasing range while still operating from a 1.6V supply.

On-chip 20b ΔΣ Digital to Analog Converters provide high-accuracy and arbitrary waveform generation, enabling precise bias profiles without off-chip components. A feedforward cancellation path prevents the electrode bias from contaminating the readout, ensuring high linearity and minimal offset in sensor currents. By chopping critical amplifier stages and carefully selecting chopping frequencies, the design significantly reduces flicker noise and electrode leakage currents. A combination of programmable transimpedance and gain stages extends the current sensing range from a few pA to hundreds of μA, achieving exceptionally high dynamic range. To handle large sensor capacitances across different samples, stability is maintained through careful loop analysis and efficient compensation. The device can duty-cycle certain blocks (like Analog to Digital Converters) to minimize power in applications needing only settled readings, while always maintaining correct sensor bias. The test chip layout can be seen in Figure 1.

Results

The test chip micrograph is shown in Figure 2. Full electrical and electrochemical characterization was run in the lab and the measured data show excellent alignment with commercial lab equipment for glucose sensing, voltammetry peak detection, and Open Circuit Potentiometry measurement. Its highly integrated architecture eliminates bulky off-chip components, lowering system cost and complexity while enhancing noise immunity. With the core area measuring only about 0.4mm² and consuming down to less than 100μW, the ASIC is well-suited for wearables, implants, IoT-based environmental monitoring, and many emerging applications. Overall, this innovative design pushes state-of-the-art boundaries with its wide bias range, high resolution, multi-method support, and low-power operation.

Our design achieves a peak SNR better than 100dB and an exceptional linearity (R^2) of about 0.999996 advancing the state of the art. The leakage current through the reference and working electrodes were measured to be less than 50pA. The overall power consumption is less than 100 μW mainly dominated by the Delta Sigma ADC. Five dies were characterized to confirm the performance metrics

Why Europractice?

As a research team, our mission is to advance integrated mixed-signal circuits and systems, which need manufacturing and validation by hardware measurements to make an impact to the community. Europractice offers the access and support to a large number of technologies, which makes our research possible at all. The mini@sic runs and various packaging options offered by Europractice are ideal for us, as limited chip size can be realized for a reasonably low cost.

Acknowledgements

This work has received funding from the Swiss State Secretariat for Education, Research, and Innovation (SERI) under the SwissChips initiative.

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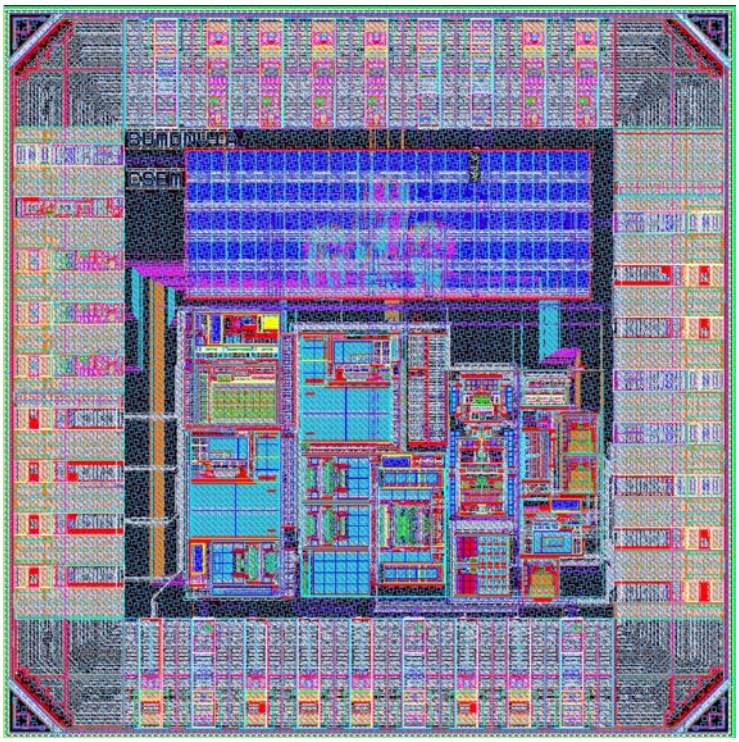

Fig.2: Micrograph of the high dynamic range and low power electrochemical analog front end testchip.

ALPACA: An Accelerator Chip for Nested Loop Programs

Friedrich-Alexander-Universität (FAU), Erlangen-Nürnberg, Germany

Contacts: Dominik Walter, Marcel Brand, Christian Heidorn, Michael Witterauf, Frank Hannig, and Jürgen Teich
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Technology: GlobalFoundries 22nm FD-SOI 22FDX
Die Size: 3.2mm x 3.125mm
Design Tools: Cadence Genus, Cadence Innovus
Application Area: Computing

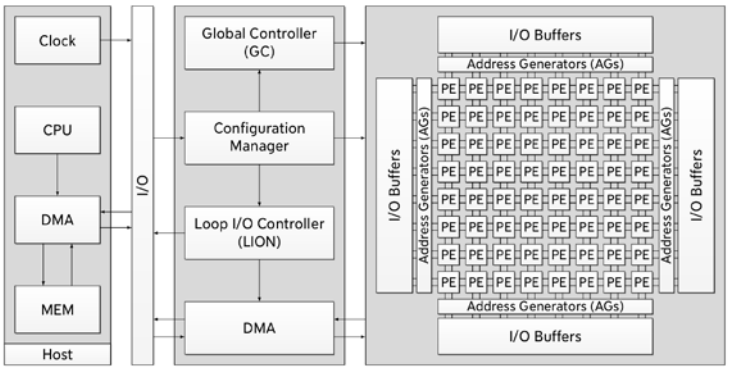

Fig.1: Overview of the ALPACA architecture. On the right, the 8×8 PE array with surrounding address generators and I/O buffers are shown. The remaining peripheral controllers are shown in the centre. A host system is shown on the left side.

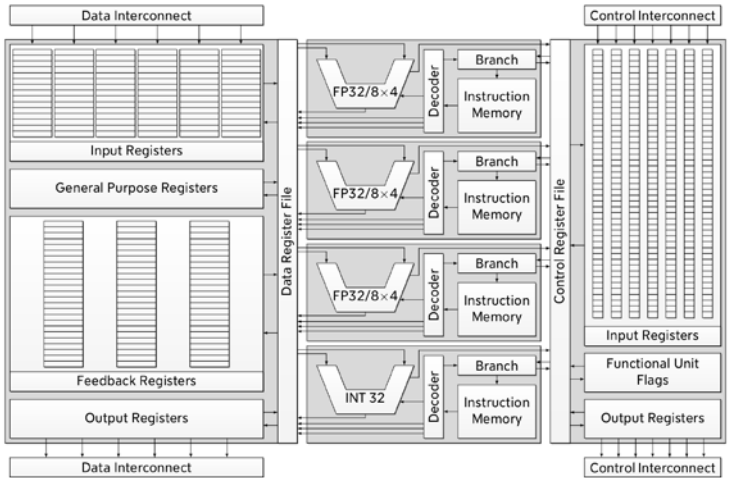

Fig.2: Architecture of a single processing element with 4 FUs (center), a control register file (right), and a data register file (left). The output registers are connected via an interconnect with the input registers of neighbouring PEs.

Introduction

In recent years, the ever-increasing demand for computing power has led to the development of a wide variety of computer architectures. They differ in many ways, each offering a trade-off between performance (e.g. giga operations per second, short GOPS) and programmability. Our processor array architecture, ALPACA [1], combines the flexibility of lightweight programmable processors with the efficiency of application-specific accelerators by executing multi-dimensional loops using a local sequential, global parallel strategy, where each PE sequentially executes all loop iterations within an assigned portion of the iteration space, while all PEs run concurrently. This approach preserves data locality and includes architectural innovations to reduce control overhead, which accounts for about two-thirds of all CPU operations in digital signal processing and scientific computing applications.

Description

Figure 1 shows the architecture of ALPACA. It implements an 8x8 Tightly-Coupled Processor Array (TCPA) [2], basically an array of small processing elements (PEs) surrounded by 4 I/O buffers containing small memory banks for input and output data.

The architecture of a PE is shown in Figure 2. It contains 4 Functional Units (FUs), shown in the centre, which support the execution of either a single-precision floating point operation or four custom 8-bit floating point operations at a time [3]. Each FU executes its own local microprogram, for which it contains a dedicated instruction memory, decoder and branch unit. This principle is known as Orthogonal Instruction Processing (OIP) [4]. In addition to the FUs, each PE also contains two local register files. The control register file, shown on the right in Figure 2, buffers control signals coming from the Global Controller (GC), shown in Figure 1. These signals trigger individual branches within the FU microprogrammes and are shared by all the PEs. This means that the entire control flow is generated only once. In addition, each PE has a data register file supporting different register types for local storage of intermediate data.

The architecture also includes other peripheral controls such as a Configuration Manager (CM), Address Generators (AGs) and a Loop I/O Controller (LION) that schedules data transfers between the I/O buffers and external memory via a dedicated DMA. Designed as a memory-coupled co-processor, a host system can offload computationally intensive loops as part of more complex application programs to the ALPACA chip by sending an array configuration to the CM for each loop to be accelerated. Once completed, it triggers the start of a parallel

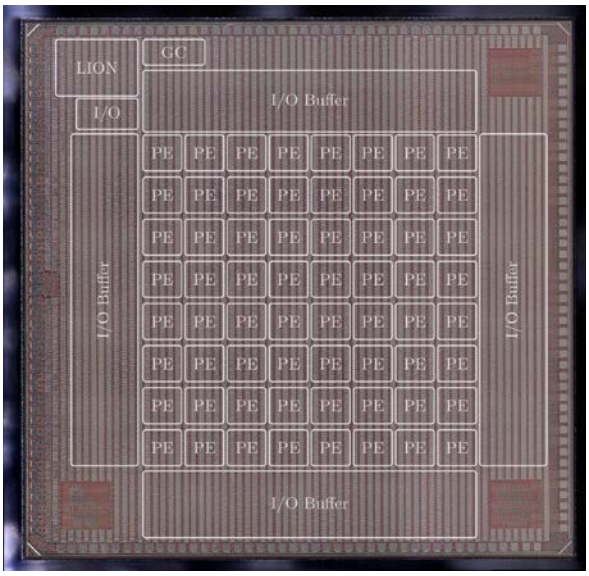

Fig.3: Die photo taken by Fraunhofer IIS. The boxes denote the placement of the corresponding component.

loop execution on the chip. The chip then independently processes the entire loop, including loading and storing I/O data.

Results

The chip has been manufactured in 22nm on a 10mm^2 die (Figure 3) and, subsequently, packaged and integrated into a testboard (Figure 4). The test board acts as an FPGA extension board by connecting the chip to the FPGA I/Os via an FMC connector. With overclocking, the highest working frequency of 700 MHz resulted in a chip performance of 538 GFLOPS. However, this design point is also the least energy-efficient one with 71.68 GFLOPS/W. In contrast, to achieve a clock frequency of 50 MHz, 0.6 V was sufficient. The observed energy efficiency was 270.42 GFLOPS/W in this case.

Why EUROPRACTICE?

Europractice enables even the smallest university teams to design and tape out complex chips successfully. The MPW runs provide an excellent opportunity to develop an idea into an affordable silicon-proven chip architecture, with Europractice providing crucial support and guidance throughout the process.

Acknowledgements

This work was funded by the Deutsche Forschungsgemeinschaft (DFG, German Research Foundation) – Project number 146371743 – TRR 89: Invasive Computing.

Special thanks also to Europractice and the Fraunhofer IIS, especially Stefan Rudischhauser and Thomas Drischel, for the extensive help and support.

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Fig.4: ALPACA test board mounted on an FPGA.

An All-Analog Neural Network Inference Accelerator with Input, Output and Weight Reuse

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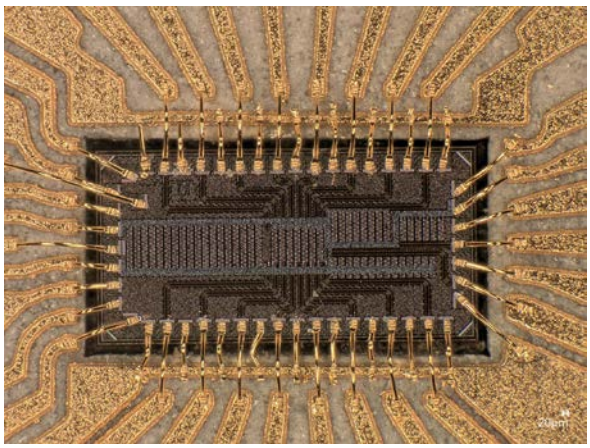
Technology: GlobalFoundries 22nm FD-SOI 22FDX
Die Size: 1mm x 2mm
Design Tools: Cadence Virtuoso, Siemens Calibre, Keysight ADS
Application Area: AI

Introduction

Artificial neural networks (ANNs) are widely used in modern applications, but their high computational demands result in significant energy consumption. This limitation makes it challenging to deploy ANNs on edge and IoT devices like smartphones and sensors. To address this issue, specialized ANN accelerators with optimized architectures and circuits have been developed. In our work, we have designed an all-analog ANN accelerator that achieves exceptional energy efficiency.

Description

The all-analog accelerator implements three ANNs with one, two and four neural layers. Depending on the task, one ANN can be selected. Each neural layer has 8 neurons and consists of analog multi-bit multiply-accumulate (MAC) cells and analog voltage-to-time converters (VTCs) with ReLU transfer function. Digital-to-Analog and Analog-to-Digital converters inbetween neural layers are fully avoided to increase the energy efficiency.



Every MAC and VTC cell can be tuned individually to calibrate mismatch for an increased compute resolution.

Results

The ANN accelerator is tested with a classification task and achieves an accuracy similar to an ideal ANN of same size and resolution. It achieves an system-level energy efficiency of 334 TOPS/W and 788 TOPS/W for the analog compute circuits only. By calibration of all computation circuits, the effective resolution increases from 2 bit to 5 bit. The clock frequency is 500 MHz.

Why Europractice?

Europractice gives us access to state-of-the-art technologies and provides the tools to design our ASIC and printed circuit boards. They offer quick and helpful support during the tape-out process. Without all this help, we would not be able to achieve our ambitious goals. We are very grateful for this and look forward to working together in the future.

Acknowledgements

The work is funded by the German Federal Ministry of Education and Research within the CELTIC-NEXT project AI-NET-ANTILLAS under grant no. 16KIS1313.

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Fig. 1: Photograph of the fabricated ASIC. It is placed in a cavity of a high-frequency printed circuit board and connected with wire bonds.

AsynCronos 1, an Asynchronous Quasi-Delay Insensitive Toggle Priority Arbiter for AER-based applications

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Contact: Anthony Krieger
E-mail: anthony.krieger@etu.unistra.fr
Technology: ST 28nm FD-SOI CMOS
Die Size: 1000µm x 1000µm
Design Tools: Cadence Virtuoso
Application Area: Datacom / Telecom

Introduction

Nowadays, Single Photon Avalanche Diode (SPAD) on standard CMOS technologies are readily available and low cost. This opens new applications for Time-Correlated Single Photon Counting (TCSPC) devices. Those use a Time to Digital Converter (TDC) to precisely measure the duration between the emission and detection of a photon. To reduce the drawbacks of SPAD or for specific applications, high number of SPADs and/or a high output rate collecting circuit is needed [1-3].

To transfer these data from several TDC to a process unit, an arbitrating unit is mandatory. The circuit collecting all the data should be easy to scale, able to sustain a high throughput, low power, small, and reliable. An asynchronous arbiter is an ideal candidate because it is fast, low power especially while idling, reliable, and easy to scale [4, 5].

Different asynchronous Priority Arbiters (PA) [6] are already available in the literature, but they always present a drawback. Fixed Priority Arbiters (FPA) are fast and simple to implement [7] but their arbitration is unfair [8], leading to data being stuck in the transfer circuit for a long period of time. Dynamic Priority Arbiters (DPA) [9-11] resolve this problem, but some are susceptible to temporal collision. Finally, all these PA use a micropipeline architecture which needs careful timing analysis and layout leading to susceptibility to Process, Voltage, and Temperature (PVT) variations. To resolve all of these problems, a new Quasi-Delay Insensitive (QDI) Toggle Priority Arbiter (TPA) was designed.

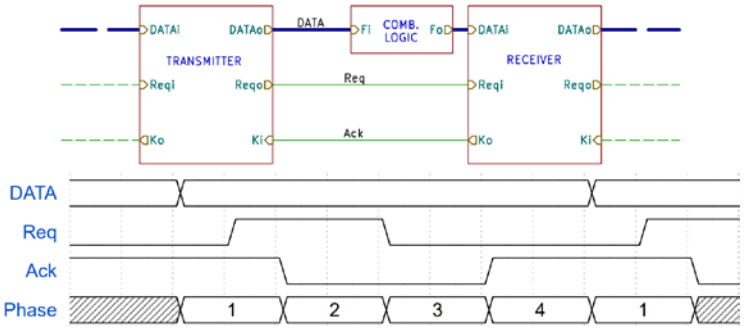

Fig.1: 4-phase protocol circuit and its chronogram.

Description

Asynchronous circuits have the advantage to be performant, emit low electromagnetic emissions (EMI), being robust towards process, voltage and temperature variations and having no clock distribution and clock skew problems [3]. These asynchronous circuits rely on a handshaking protocol, which is presented in Figure 1. One register sends to the next one some data with a request. The second register can then sample the data and respond with an acknowledgment. The data, request and acknowledgment can be taken back and a new cycle can restart. One major drawback of this implementation is that the request signal must always arrive after the data, which requires meticulous timing analysis and layout.

To overcome this drawback, one can use a QDI protocol like Dual-Rail [4], in which one bit is encoded with two mutually exclusive wires D0 and D1. With this method, the request is directly encoded into the data and therefore there is no more need for a matched delay on the request line. Two data are separated by a NULL value to pace the system.

Address Event Representation was first proposed by [12] and is used to transfer several inputs into one output. At each stage, an arbitration is done between two (or more) different inputs to select the one to transfer at the arbiter's output with an added address to indicate the origin of the data. By cascading several arbiters, one can create a Data Path Tree (DPT) with a large amount of inputs.

Two of the main challenges in the TPA's design are to ensure that no data are lost, especially when two requests are sent at the same arbiter in a small time window, and achieve a toggling priority. Those two can be achieved hence to a MUTEX or mutual exclusive element. It ensures that only one of the requests can access the arbiter at the same time. The behaviour of the MUTEX can be seen in Figure 2.

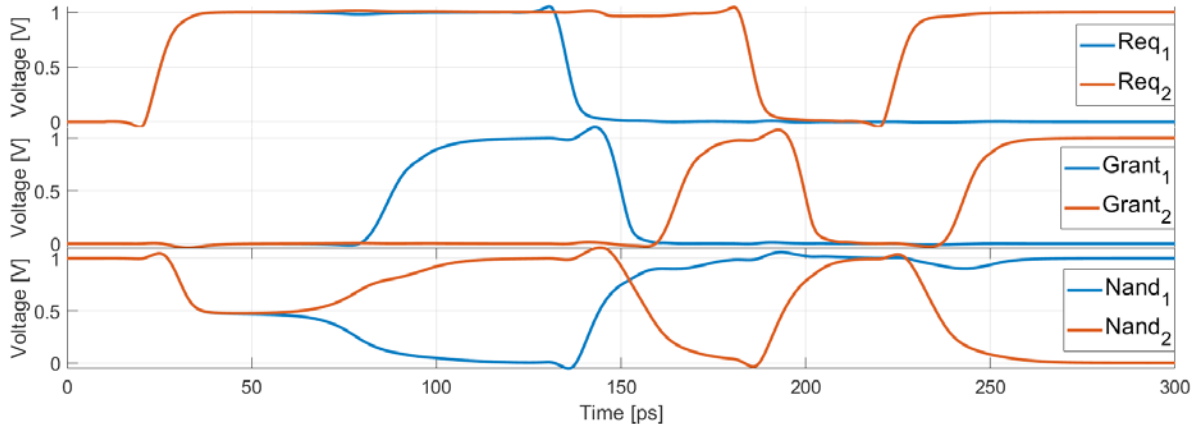

Fig.2: MUTEX simulation in 28 nm FD-SOI.

The AsynCronos 1 chip, shown in Figure 3, incorporates several tests to characterize all the key parts of this new QDI TPA. Tests of the Dual-Rail Registers are set up to measure their speed and power consumption. Next, the MUTEX, responsible for the toggle behaviour of the arbiter and for the lossless data transfer, is tested to measure its robustness and delay (precision +- 3 ps) in case of two simultaneous request. Through these results, we will be able to measure the possible added delay caused by metastable states and compare it to the total delay of the circuit. Then, the delay, frequency and power consumption of a 16 to 1 DPT will be precisely measured (+-100 ps). Finally, the output data of a 256 to 1 DPT will be checked to ensure flawless data transfer and encoding of the TPA.

Results

The circuit has been received recently and has yet to be tested.

Why Europractice?

ICube has been using the Europractice services via CIME-P for several years. This choice is driven by good support and assistance and the access to cutting edge technology, in this case, FD-SOI 28 nm.

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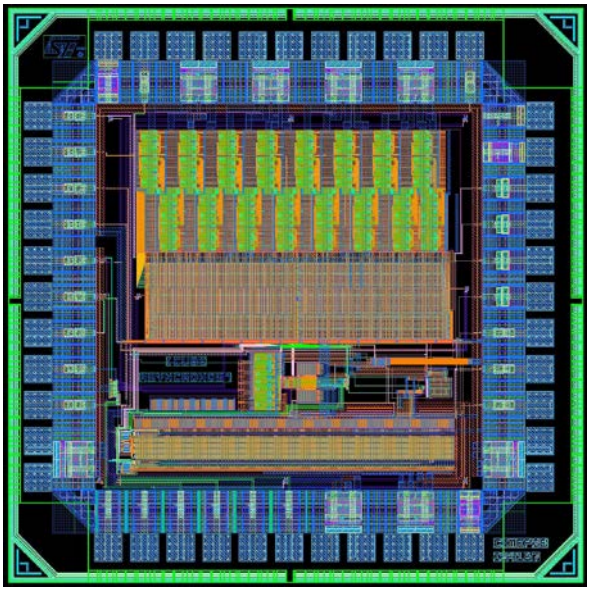

Fig.3: AsynCronos 1 layout.

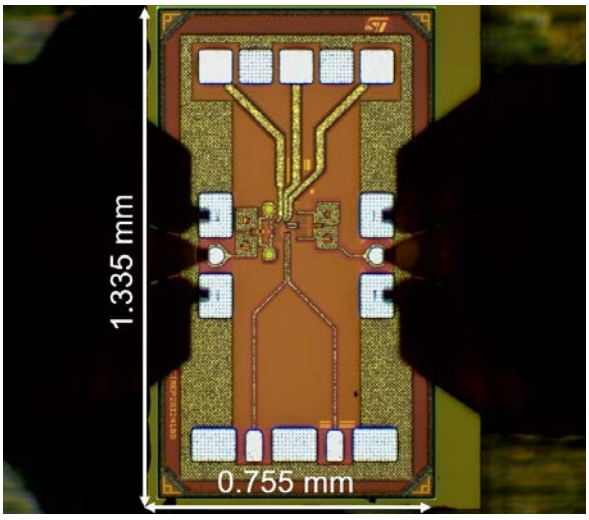

Fig.1: Micrograph of fabricated active analog downconverter.

Analog Downconverter for 6G Applications

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Contacts:	Mantas Sakalas, Eidvidas Šatkauskas
E-mail:	mantas.sakalas@bpti.eu
Technology:	ST 28nm FD-SOI CMOS
Die Size:	1.335mm x 0.755mm
Application Area:	Datacom / Telecom

Introduction

HERMES project aims to develop a 6G licensed band transceiver by using advanced CMOS technology in fusion with artificial intelligence. Analog downconvertion mixer is designed as a part in receiver chain.

Description

The developed analog downconvertion mixer is depicted in Figure 1. It was designed to translate the RF frequency from (141-164) GHz to (0.1-10) GHz IF frequency range. Active downconvertion mixer is based on double-balanced Gilbert cell topology with emphasis to provide suppression of spurious mixing products and improve isolation between the ports.

Results

Figure 2 illustrates the measured conversion gain CG and noise figure NF in RF frequency range of (141-164) GHz. The minimal conversion loss is approximately 6 dB with 3 dB-bandwidth of 25 GHz. The minimal (double side-band) noise figure of 15,5 dB value is achieved when terminating to 50 ohm.

Why Europractice?

Europractice helps to push independent researchers to innovate and facilitate their ideas by providing access to various MPW runs. Our company is impressed by the level of customer support and great communication practices.

Acknowledgements

This design is part of the HERMES project, that received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 964246.

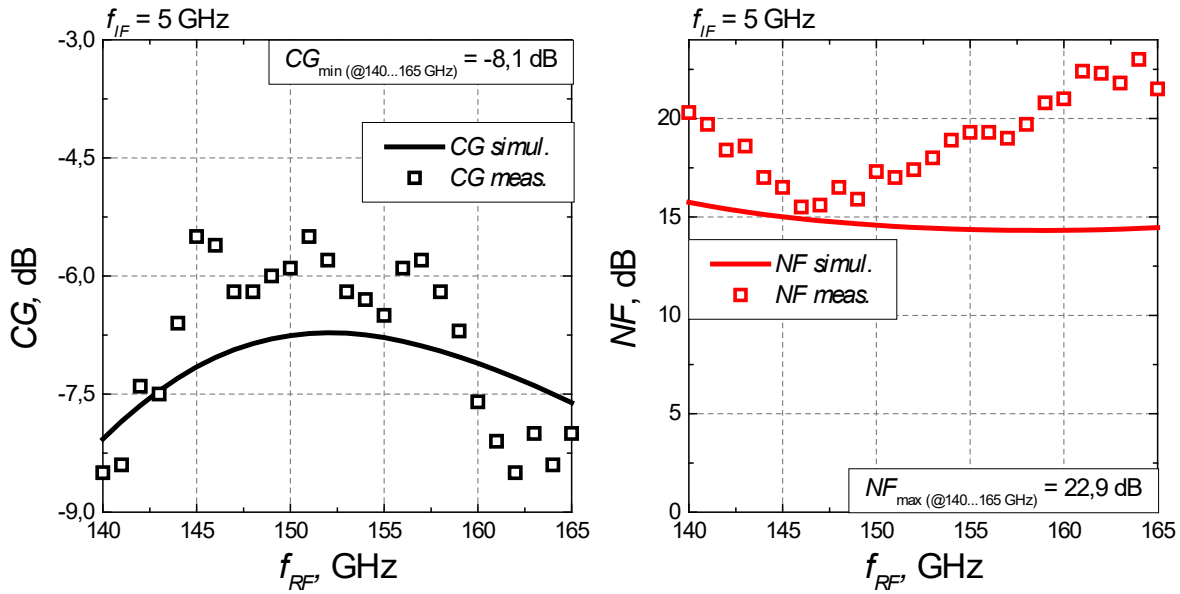

Fig.2: Manufactured downconverter simulated (line) and measured (scatter) conversion gain CG and noise figure NF dependence on input frequency fRF, output frequency is fixed at fIF = 5 GHz.

Warm front-end for X-ray cryogenic detectors

APC Laboratory, Paris, France

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Technology:	ST 130 nm SiGe BiCMOS9MW
Die Size:	AwaXe_v4.5_LNA: 1.56mm x 2.25mm; AwaXe_v4.5_DAC: 2.69mm x 1.75mm; AwaXe_v5_FC: 2.4mm x 0.92mm; AwaXe_v5_DF: 2.3mm x 1.1mm
Application Area:	(Aero)Space

Introduction

AwaXe_v4.5s and v5 (Athena Warm Asic for the X-IFU Electronics – proto versions) are prototype ASICs developed for the Warm Front End Electronics (WFEE) of the ATHENA X-ray observatory. It is dedicated to validate the use of the ST BiCMOS technology for the readout of the X-IFU (X-ray Integral Field Unit) instrument of the ATHENA ESA space telescope.

AwaXe_v4.5 are for testing low noise amplification (LNA) and bias (current DACs) of a cryogenic detection chain based on TES/SQUID superconducting devices.

AwaXe_v5 are operating RS485/I2C series-bus required for the on-chip controls of the DACs. Different radhard by design were tested for the digital library to garanty radiation robustness.

These ASICs belong to the "AwaXe and SQmux ASIC families" developed at APC Laboratory for SQUID/TES readout.

Description

AwaXe ASICs are developed for the readout (analog/mixed LNA/DAC) and the adjustment (digital/mixed I2C decoders/ RS485 driver) of the X-IFU instrument.

- AwaXe_v4.5_LNA: 4 fully-differential Low Noise Amplifiers, with 160 V/V gain, DC to 40 MHz bandwidth, 0.7 nV/√Hz input noise, 250 ppm/K gain drift and 2 Vpp output dynamic range. Two of them include an offset compensation., and two also include the Rptat resistor used to set the LNA current bias.
- AwaXe_v4.5_DAC: 4 differential configurable milli-ampere current sources of 10-bits for the bias of SQUIDs and TES (superconducting devices), and also for the offset compensation of the LNA. Current noise, as low as 20 pA/√Hz, has been optimized down to low frequencies.
- AwaXe_v5_FC: A digital RadHard series bus RS485/I2C with two layers of address, for the slow control of the WFEE. A full-custom library has been developed with double guard ring surrounding all the NMOS and all the PMOS.
- AwaXe_v5_DF: A second digital RadHard ASIC dedicated to the series bus I2C of the WFEE, also with two layers of address. This ASIC was developed using digital flow method by the WEEROC company.

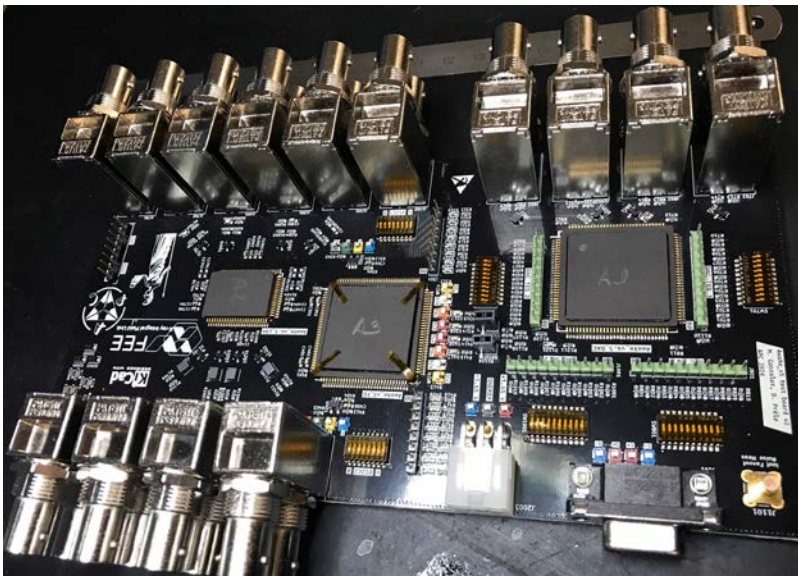

Fig.1: Photo of the test board.

Results

LNAs exhibits input voltage noise below 0.7nV/√Hz. Here, the measurement is dominated by the room temperature representative sensors.

Why Europractice?

Our ASICs mainly apply ST 130nm SiGe technology or ams OSRAM 350 SiGe technology proposed by the MPW Europractice services via CIME-P in France.

Acknowledgements

The development is funded by ESA, CNES and CNRS.

References

[1] Si Chen, Damien Prêle, Manuel Gonzalez, Jean Mesquida, Bernard Courty, et al.. , "ASIC design evolution of ATHENA X-IFU warm front-end electronics", SPIE Astronomical Telescopes + Instrumentation 2024.

An 8.4-to-11.1 GHz ADPLL for Automotive Applications

Integrated Analog Circuits and RF Systems, RWTH Aachen University, Aachen, Germany

Contacts:	Tim Lauber, Johannes Kuhn, Kenny Vohl, Lantao Wang, Ralf Wunderlich, Stefan Heinen
E-mail:	ias@rwth-aachen.de
Technology:	TSMC 28nm HPC+
Die Size:	1.217mm x 1.217mm
Design Tools:	Cadence Virtuoso, Spectre RF, Genus, Innovus, Xcelium
Application Area:	Automotive / Transport

Introduction

In modern wireline and wireless communication standards, high-quality clock signals are essential for reliable error-free communication at very high data rates. This creates the need for low phase noise LOs, typically realized by PLLs. Classic implementations of PLLs are in the analog domain, based on a charge pump and RC loop filter. With decreasing CMOS node sizes, scaling of analog circuits poses significant challenges due to reduced supply voltages, higher leakage currents and short channel effects of the devices. On the other hand however, with increased transit frequencies and smaller devices, digital intensive circuits becoming more and more attractive. Therefore, the All-Digital Phase-Locked-Loop (ADPLL) becomes the preferred choice over the traditional analog PLL in modern CMOS nodes. Further benefits are smaller area, the possibility of extensive digital calibration and programmability, as well as portability to other technologies.

Description

The presented design consists of a low-noise ADPLL, synthesizing a variable frequency between 8.2 and 11.1 GHz. A class-C digitally controlled oscillator (DCO) with a fine resolution of 40kHz is used for generation of the variable frequency [1]. The phase detection is performed by an accumulator for the integer part and a high-resolution 2D-Vernier time-to-digital converter (TDC) for the fractional part of the phase [2]. In order to compensate PVT effects and ensure linear operation, the TDC features an integrated calibration scheme. The reference frequency is generated using an integrated crystal oscillator. All the other parts of the loop are fully synthesized from HDL description.

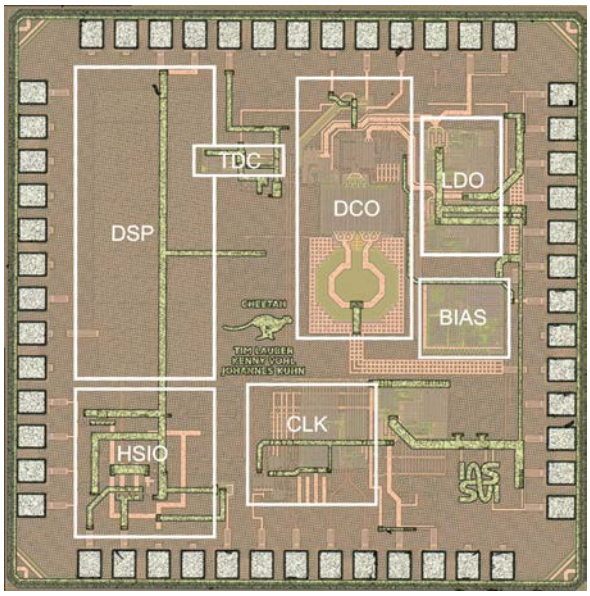

Fig.1: Chip Micrograph

In order to debug the digital-intensive loop of the ADPLL, a 1Gbps debug interface is integrated on the chip, allowing real-time monitoring and configuration of digital control signals.

Results

Figure 2 shows the transfer curve of an 8-bit controllable delay cell inside the TDC. The delay cell is controlled by the delay control word (DCW) in order to be set to an appropriate delay by the integrated calibration algorithm. Since the upper four bits are being used for coarse tuning, while the lower four bits are used for fine tuning, a staircase-like behavior can be observed. The yellow, green and red lines show simulation

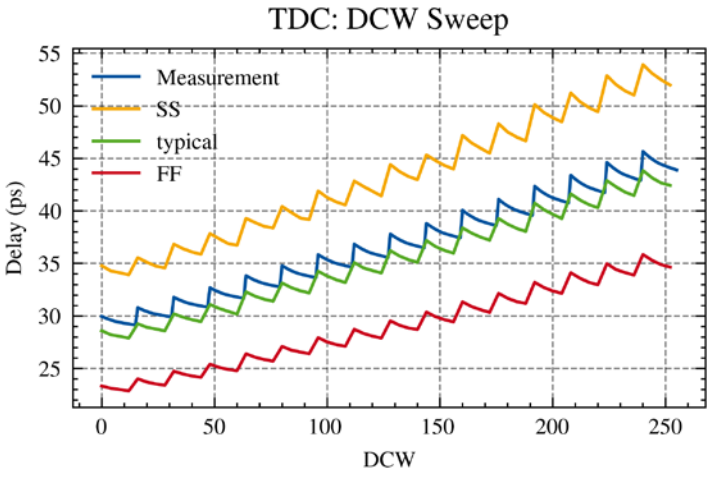

Fig.2: TDC Delay Cell measurement

results of post-layout simulations for the slow-slow, typical and fast-fast corner, respectively. The blue curve results from lab measurements for one sample. The measurement result matches very well with the simulated values and thus proves the high accuracy of the models provided by Europractice.

Why Europractice?

With Europractice's services, universities and research groups have the opportunity for on-silicon prototyping at affordable cost. This includes the access to industry standard EDA software and the mini@sic program, which offers access to state-of-the-art nanoscale technologies from leading foundries such as TSMC HPC+ 28nm.

Acknowledgements

We would like to express our gratitude to Europractice and imec for their excellent support during this tapeout and throughout the last years.
This work was supported by the German Federal Ministry of Education and Research through the Project KI4Boardnet under Grant FKZ 16ME0780.

References

[1] L. Wang et al., "A 28 nm 8.2-11.1 GHz Class-C Digitally Controlled Oscillator with 40 kHz Tuning Resolution," 2024 IEEE International Symposium on Circuits and Systems (ISCAS), Singapore, Singapore, 2024

[2] T. Lauber, L. Wang, J. Bastl, K. Vohl, R. Wunderlich and S. Heinen, "A TDC With Integrated Snapshot Circuit and Calibration in 28-nm CMOS," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 71, no. 3, pp. 1581-1585, March 2024

Wideband Mixer-First Receiver for 5G Application

Silicon Austria Labs (SAL) GmbH, Austria

Contact: Fatemeh Abbassi
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Technology: TSMC 28nm HPC(+)
Die Size: 1mm x 1mm
Application Area: Datacom / Telecom

Introduction

The rapid evolution of 5G wireless communication and the push toward beyond-5G technologies have introduced significant challenges for receiver front-end design. These include achieving wideband operation, high linearity, low noise figure, and reconfigurability. With 5G networks spanning frequencies from sub-6 GHz to millimeter-wave (mmWave) bands, versatile and efficient receiver architectures are essential to support the increasing demand for wider bandwidth channels and higher data rates.
This work presents the design and implementation of a reconfigurable 2–30 GHz in-phase and quadrature (IQ) receiver in 28-nm TSMC CMOS technology, addressing these challenges.

Description

Figure 1 shows the die micrograph of the chip, which includes two versions of a mixer-first receiver front-end implemented in 28-nm TSMC CMOS technology. This receiver architecture downconverts the RF signal using a series switch mixer topology. The resulting baseband signal is then amplified using a baseband amplifier and a 50-Ohm driver buffer.
To enhance linearity, feedback linearization was applied at the baseband stage, albeit at the expense of increased noise. An innovative approach utilizing a series mixer was introduced, enabling the use of a 50% overlapping LO signal over a wide frequency range. Additionally, a wideband digital method was implemented for IQ LO signal generation, resulting in a unique circuit design capable of operating seamlessly across the two primary frequency bands of 5G systems.

Results

The proposed mixer-first IQ receiver demonstrates excellent reconfigurability and performance across both sub-6 GHz and mmWave bands. It offers adjustable conversion gain ranging from 10 to 30 dB, and the intermediate frequency (IF) bandwidth is tunable between 70 and 500 MHz. The circuit consumes 35mW from 1.2V supply.

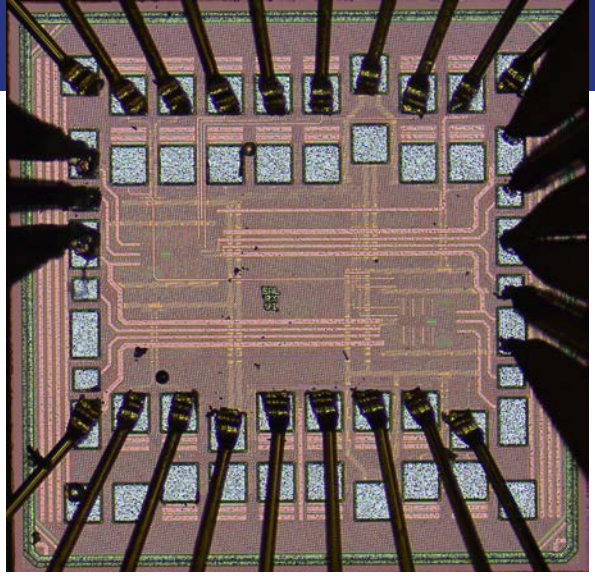

Fig.1: Die micrograph of receiver front-end

The fabricated device (Figure 1) was characterized using a custom-designed PCB, wire-bonded to DC supplies and IF signal interfaces, with a probe station used to apply RF and LO signals. The measurement results show that the design goals were successfully achieved.

The DC performance of the device was evaluated and found to closely align with the simulation results. In addition, the S-parameters and AC performance of the chip were measured. The measurements confirm the simulation predictions for gain, bandwidth, and linearity across the target frequency range, with a reasonable deviation.

Why Europractice?

Europractice provides an excellent platform for universities and research institutes to turn innovative ideas into reality. They offer affordable pricing and fast processing times, which are highly beneficial for research projects.

One of their key offers is the mini@sic runs, which allow researchers with smaller design requirements to fabricate their chips at a low cost without needing to reserve large silicon areas. In addition, Europractice supports a wide range of technologies, giving researchers access to various fabrication processes to suit their needs. Their staff is also highly responsive and supportive, ensuring a smooth and efficient experience for users at every stage of the project.

Acknowledgements

This work has been supported by the "University SAL Labs" initiative of Silicon Austria Labs (SAL) and its Austrian partner universities for applied fundamental research for electronic-based systems.

References

F. Abbassi, T. Ostermann and C. Wagner, "Enhanced Mixer-First Receiver Using Series Switch N-Path Passive Mixer for Millimeter-Wave 5G Applications," 2024 IEEE Nordic Circuits and Systems Conference (NorCAS), Lund, Sweden, 2024, pp. 1-5, doi: 10.1109/NorCAS64408.2024.10752447.

ColorPix: A front-end ASIC for color imaging

Czech Technical University in Prague, Czech Republic

Contacts: Josef Gecnuk, Zdenko Janoska, Jakub Jirsa, Lukas Tomasek, Pavel Vancura
E-mails: zdenko.janoska@fjfi.cvut.cz

Technology: TSMC 65nm
Die Size: 3000µm × 5000µm
Design Tools: Cadence
Application Area: High Energy Physics (HEP)

Introduction

X-ray color imaging is a promising method for medical imaging and non-destructive testing. ColorPix (Figure 1) uses photon-counting hybrid detectors with multiple threshold levels. To enhance the spatial resolution of the detectors, a shrinking of pixel size is needed. With decreasing pixel pitch size, charge sharing and fluorescent photons cause the charge spread across the pixel matrix. Therefore, on-chip algorithms with inter-pixel communication are needed to compensate for these effects.

Description

ColorPix is a hybrid active pixel sensor with a 32x32 pixel matrix (Figure 2). Dimensions of pixels are 70x70µm. Sensitive area is 2.2 x 2.2 mm. The detector can operate in multiple modes: multi, mono and custom color mode. Readout digital part offers 3.2 Gbit interface. The signal produced by incoming photons is amplified using Charge Sensitive Amplifier (CSA). The output signal is then dived into two branches: Digital and Analog. Digital branch starts with pixel discriminator which signalize whether the pixel collected some charge or not, the output of pixel discriminator is connected to pixel digital logic. Digital logic is responsible for inter-pixel communication (cluster formation) and sampling. Analog branch follows by Peak detector and hold circuit (PDH) which memorize the maximum value of CSA. Next the Operational Transconductance amplifier which converts the PDH output signal to current. Finally the multi-threshold window discriminator performs the digitization which of the counter should be incremented.

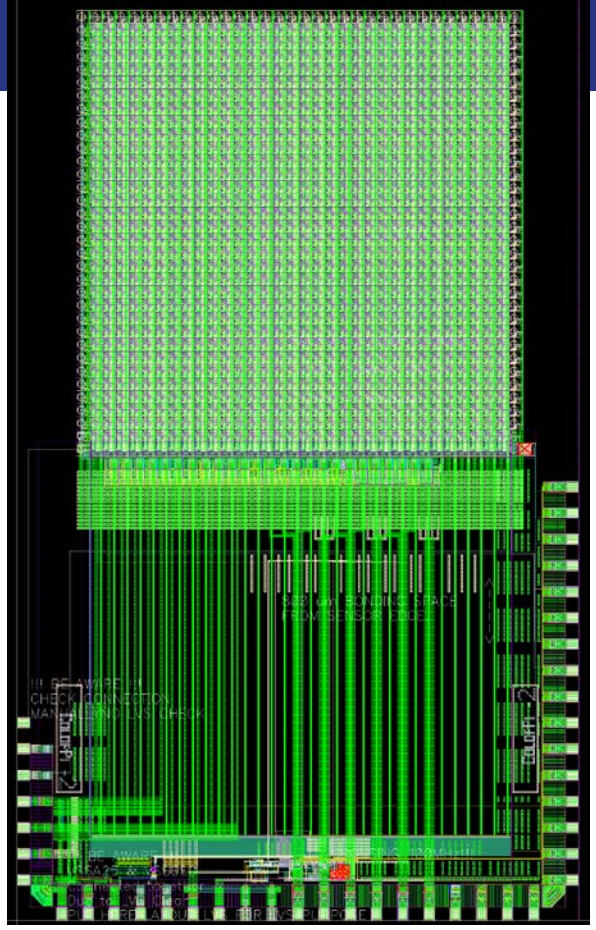

Fig.1: Layout of ColorPix.

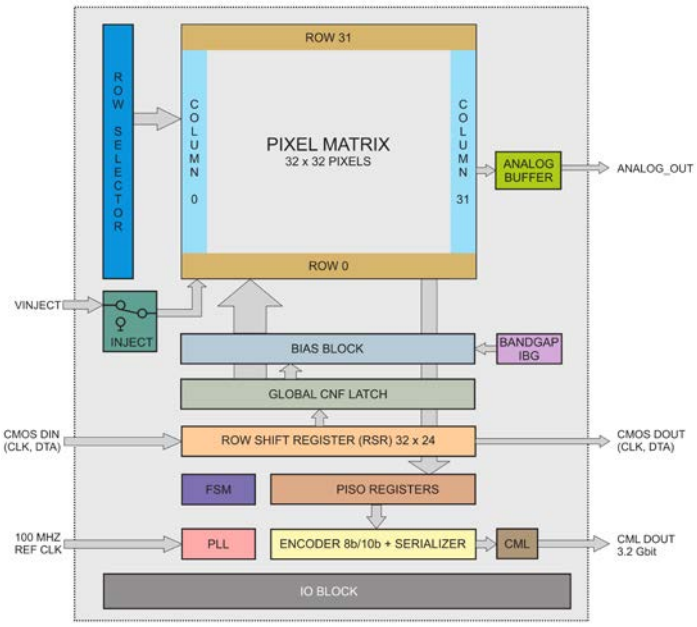

Fig.2: ColorPix block diagram.

Results

The electrical test were performed to verify functionality of the chip. First results showed that the internal PLL and digital readout blocks are fully operational. The Monte Carlo simulation (Figure 3) was done with two configurations: 1. charge summing algorithm turned on; 2. charge summing algorithm turned off.

Why Europractice?

Our research group is cooperating with Europractice for several years already. Europractice partner imec provides excellent technical support, which is crucial for successful submission of designs. Imec is also very helpful with all the administrative issues. The staff is very responsive and highly qualified. Thanks to Europractice we have access to different technologies at an affordable price.

Acknowledgements

The work was supported from European Regional Development Fund-Project "Center of Advanced Applied Science" No. CZ.02.1.01/0.0/0.0/16-019/0000778 and by the Grant Agency of the Czech Technical University in Prague, grant No. SGS20/175/OHK3/3T/13.

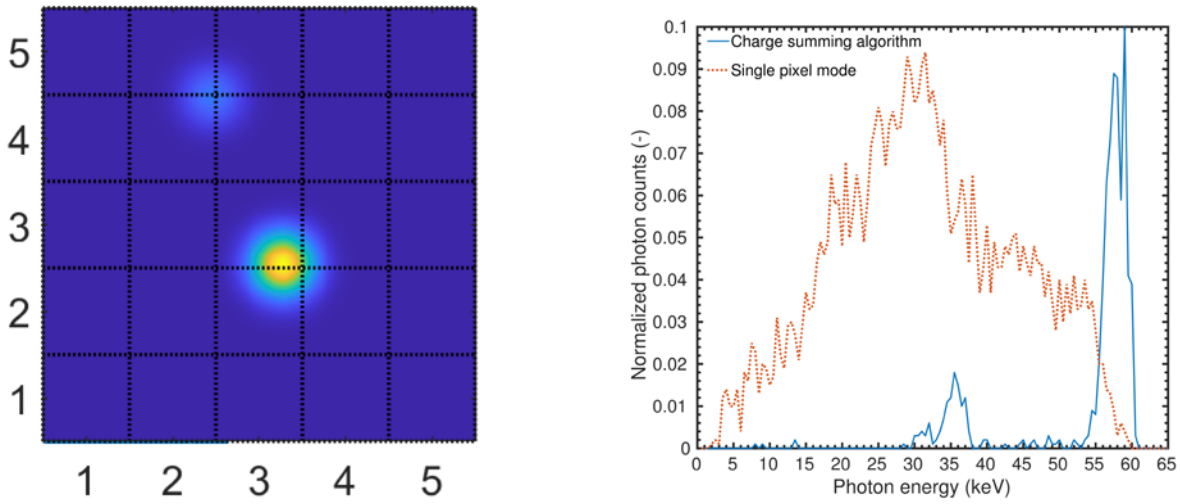

Fig.3: (Left) e– density at collection electrodes after X-ray photon interaction (Right) Normalized photon counts at central pixel in single pixel mode (red) and charge summing mode (blue).

Smartmini: Design of 18-bit Delta-Sigma Modulator

IC'Alps, Saint-Martin-d'Hères, France – University of Pavia, Pavia, Italy

Contacts:	Christophe Gaillard, Adrien Crochet
E-mail:	christophe.gaillard@icalps.com
Technology:	TSMC 65nm LP
Die Size:	1mm x 1 mm
Application Area:	Medical / Health

Introduction

This device is part of our internal R&D program (Smartmini) aiming at developing our IP portfolio for low power sensor applications. This work was also supporting a PhD thesis in the frame of an agreement with the University of Pavia (department of industrial and information engineering).

Description

The device is a second order feed-forward ΣΔ Modulator, targeting a 110 dB dynamic range, 100 dB THD, with 1 kHz signal band.

The power consumption is under 200uW @ 1.2V.

Among other constraints, the device needed to have minimised input capacitance in order to facilitate the system integration (especially for the ADC signal driving amplifier), and the architecture should facilitate the migration in various technology nodes (relax constraints on building block specifications).

The modulator has an autozeroing mechanism in order to cancel out flicker noise and offset. This is important for preserving high dynamic range for low-frequency signals.

The test chip has been designed in TSMC 65nm LP and uses only standard primitive devices. The layout is shown in Figure 1.

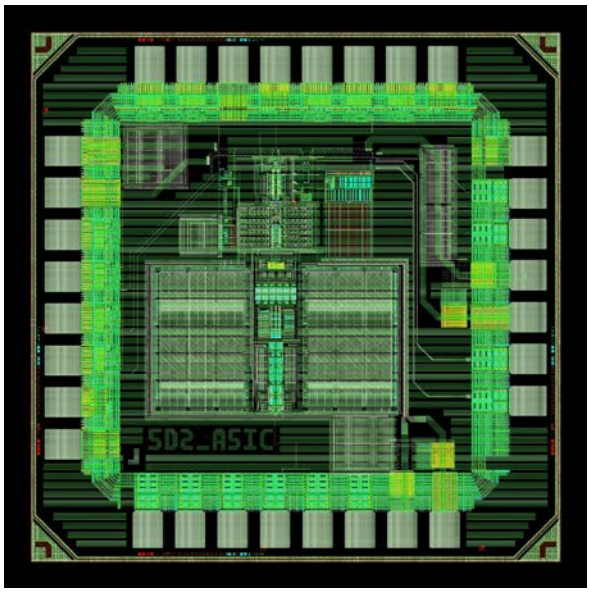

Fig.1: Test chip layout in TSMC 65 nm LP.

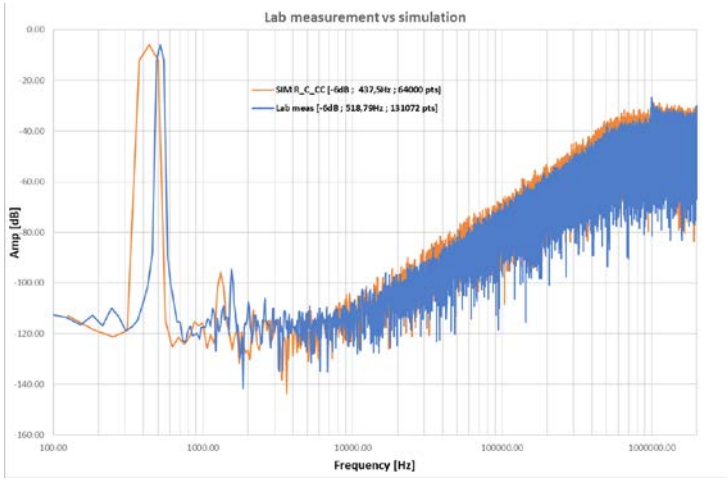

Fig.2: FFT plot simulation vs lab measurements.

Results

The chip has been tested in our characterisation lab and has shown excellent compliance with simulations, as shown in Figure 2. Signal, noise and harmonic (H3, out of band) amplitudes are very well in agreement with the simulations.

The overall performances are pretty close to the desired targets, with layout-related improvements identified for future usage.

The device is fully useable for integration in low voltage sensor interfaces (accelerometers, medical imaging, temperature, biopotentials, etc.).

Why Europractice?

Europractice was selected for its attractive MPW offering (mini@sic), while providing excellent PDK and technical support.

References

F. Torri, T. Vergine, P. Malcovati and A. Baschirotto, "Analog Techniques for Low-power High-Performance Switched-Capacitor Sigma-Delta Modulators," 2023 30th IEEE International Conference on Electronics, Circuits and Systems (ICECS), Istanbul, Turkiye, 2023, pp. 1-4, doi: 10.1109/ICECS58634.2023.10382811.

Europractice brings DARE technology to space

imec, Leuven, Belgium –
Frontgrade Gaisler, Gothenburg, Sweden

Contact: Marcel van de Burgwal
E-mail: marcel.vandeburgwal@imec.be
Technology: TSMC 65nm RF LP
Die Size: 7mm x 7mm
Design Tools: Cadence (analog, digital and mixed signal)
Application Area: (Aero)Space

Introduction

The DARE65 Demonstrator ASIC showcases all functionality available in the DARE65T radiation hardened platform. It is used to validate the suitability of the mixed signal libraries for developing flight model ASICs, with aerospace grade robustness.

Description

Imec and Gaisler worked together on the development of the DARE65 Demonstrator ASIC. The System-on-Chip consists of a LEON5 fault-tolerant CPU, onboard L1 and L2 caches and a wide variety of peripherals targeting space interface protocols (e.g. Space Wire, Space Fibre, CAN and FPGA scrubbing). Implemented with imec's full-custom DARE65T ASIC libraries for TSMC 65nm RF/LP, the device measures about 7x7mm^2 and is assembled by Kyocera on a custom organic 625-pin LGA developed by Europractice package design team.

Results

A batch of 100 samples was blindly assembled and functional testing has shown excellent yield. Out of the first set of 30 samples, only one was rejected during testing.

Different types of radiation testing were performed to emulate the harsh environments encountered in flight mode. Single Event Effects (SEE) testing uses an ionized beam to introduce transient and permanent errors in the circuit. To be able to perform this testing, 10 assembled devices were ground down to 50um thickness. Thanks to the rigid package design, utilizing a stiffener ring to ensure the total stress on the device remains limited, the thinned samples were tested and approved, showing very similar results to earlier DARE65T test vehicles.

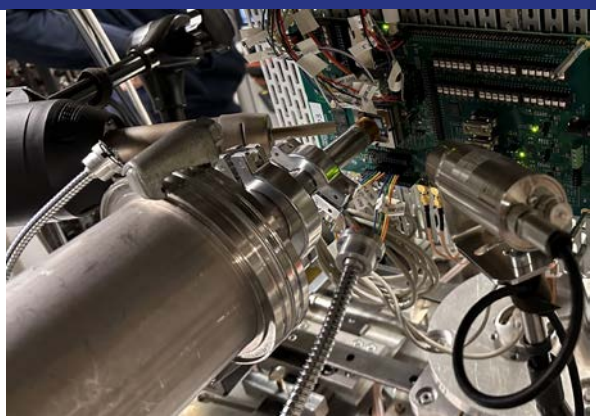

Fig.1: SEE testing of the grinded samples, with lid removed for bare die access.

Why Europractice?

Thanks to the Europractice MPW services, we could find the best trade-off between maximizing die functionality and minimizing the project budget. The Europractice team is of great support for technology access, support, manufacturing readiness assessments as well as package design, manufacturing, and assembly. They take responsibility for all supplier interactions, allowing us to focus on our core skills and bring the project to a success together.

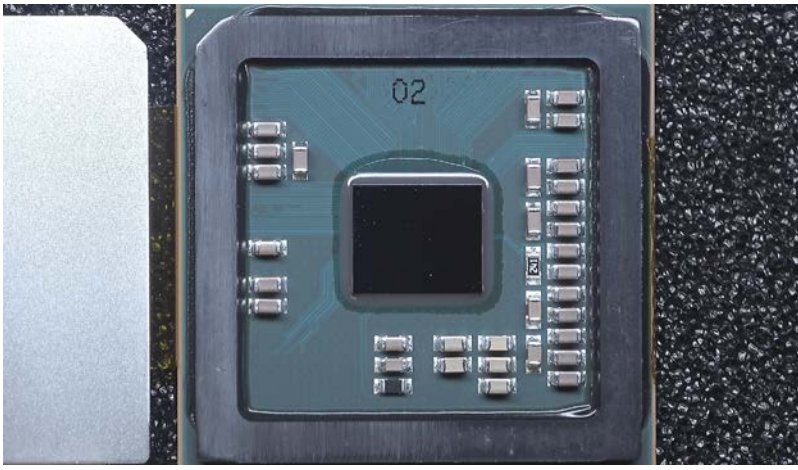

Fig.2: Detailed picture of the die after assembly on the custom organize substrate.

Acknowledgements

The DARE65 Demonstrator ASIC is funded through the ESA DARE65 activity (ESA Contract No 4000117214/16/NL/LF) under supervision of ESA's technical officer Boris Glass.
Frontgrade Gaisler has contributed greatly to the design and test of the DARE65T Demonstrator ASIC.

References

Validation, characterization and irradiation testing of the DARE65T platform. M. van de Burgwal, E. Boufouss, B. Vignon, L. Berti, G. Thys, M. Kakoulin. AMICSA 2022

UIB Neuron Microchip

Electronic Tecnology Group GEE, University of the Balearic Islands (UIB), Palma, Spain

Contacts:	M. Roca, J. Rosselló
E-mail:	miquel.roca@uib.es, j.rossello@uib.es
Technology:	UMC L180
Die Size:	1.5mmx1.5mm
Design Tools:	Cadence Genus, Synopsis
Application Area:	IoT

Introduction

Artificial intelligence poses a significant challenge for IoT applications, where algorithms and hardware must be optimised for ultra-low power consumption. This need is especially critical for battery-free edge devices, which often generate large volumes of data and therefore face communication bottlenecks when transmitting to main servers. In this context, simple neural networks and unconventional computing algorithms offer highly efficient solutions.

In our designed and fabricated microchip, we implemented a Morphological Neural Network (MNN) using Stochastic Computing for handwritten digits recognition. The results demonstrate both the accuracy and energy efficiency of the proposed approach.

Description

The designed integrated circuit implements a MNN that includes a total of 25.408 pre-configured synapses. MNNs utilise tropical algebra, where some Multiply-Accumulate blocks are replaced by addition and maximum/minimum operations. Our design also incorporates stochastic computing, so that multiplication, minimum, and the maximum operations can be performed using minimal logic gates (using XNOR, AND and OR gates for each operation respectively). This simplification greatly reduces circuit complexity—especially compared to conventional multipliers—and significantly lowers power consumption, thereby extending the operating lifetime of battery-powered systems. However, the use of stochastic computing introduces a delay in the circuit's response time, as a certain interval is required to integrate the computational results. To further decrease complexity while maintaining a high level of accuracy, the proposed neural network applies a pruning process to reduce the number of parameters generated during training, along with approximate adders that preserve detection performance.

The network is evaluated on the MNIST dataset, which contains 70,000 images (60,000 for training and 10,000 for testing). Experimental results highlight the efficiency and practicality of our approach for low-power, high-accuracy pattern recognition.

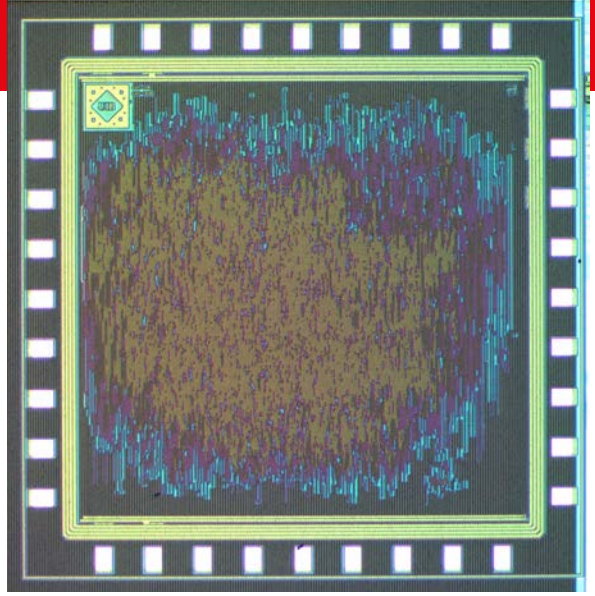

Fig.1: 180 nm UMC CMOS chip fabricated including the morphological neural network based on stochastic computing strategy.

Results

The experimental results obtained through electronic measurements on the fabricated circuit (UMC180 CMOS technology) show a high degree of efficiency. An energy efficiency of 0.11 Synaptic Operations (SOPs) per pico-joule, and a Normalized Throughput of 69.8 MSOP/(s mm^2 MHZ). For a normal operation of 100 images recognized per second, the power consumption is of the order of 40 micro-watts, and a test accuracy of 91.2% measured on the chip fabricated (with core area of only 1.4 mm^2). These results are competitive with other VLSI implementations found in the literature [1-3].

Why Europractice?

Using the UMC 180 CMOS fabrication process through Europractice was key for the development of this project since it allows fast feedback between the design and the experimental results to validate such design at a reasonable price. Also, Europractice provided us with the design tools needed to develop our designs.

Acknowledgements

This work was partially supported by the Spanish Ministry of Science and Innovation (MCIN) and the European Union NextGenerationEU/PRTR under grants PID2020-120075RB-I00 and PDC2021-121847-I00, both funded by MCIN/AEI/10.13039/501100011033 and the European Union

References

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[2] Modaresi, Farhad; Guthaus, Matthew; Eshraghian, Jason K. Openspike: An openram snn accelerator. In 2023 IEEE International Symposium on Circuits and Systems (ISCAS). IEEE, 2023. p. 1-5.

[3] Liu, Yanchen, et al. Application of deep compression technique in spiking neural network chip. IEEE transactions on biomedical circuits and systems, 2019, vol. 14, no 2, p. 274-282.

A Spintronic Based Wireless Sensor Node

Aarhus University, Aarhus, Denmark

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E-mails:	hossein.esmailbeygi@ece.au.dk, Elham.hatamzadeh@ece.au.dk, moradi@ece.au.dk
Technology:	X-FAB XH018
Die Size:	3.14mm x 1.55mm
Design Tools:	Cadence Virtuoso
Application Area:	IoT

Introduction

Wireless sensor nodes (WSN) are an essential part of any IoT system, and decreasing their power consumption reduces the total energy consumption of the network. Besides employing new circuit techniques, technology advances can improve the performance of WSNs. Recent studies show that spintronic devices exhibit promising features such as highly sensitive magnetic field sensing, which can be exploited to implement low-power WSNs. In this prototype, by combining a spintronic-based magnetic sensor (a magnetic tunnel junction - MTJ - bridge in this project) and a CMOS interface, a power-efficient WSN was implemented with the lowest FOM among all digital output magnetometers.

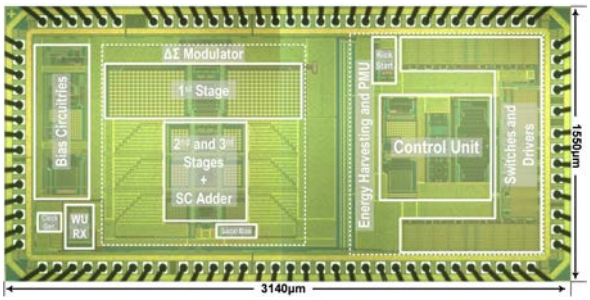

Fig.2: Die micrograph of the fabricated WSN

Description

Figure 1 shows the block diagram of the implemented WSN. This system includes a third-order CIFF delta-sigma modulator (DSM) with a single-bit quantizer and a modified switched capacitor adder, in which an 8.4pF capacitor was employed in the sampling network to acquire the sensor data. In order to sample the input signal without degrading the accuracy of the system, the sensor bridge was realized using 50KΩ MTJs to ensure that the input signal settles to its final value within more than 18-bit accuracy at the end of the sampling phase (fS=102.4KHz), consuming 45µW with 1.25V reference voltage at 1.8V supply which is 1–2 orders of magnitude lower than the required power to drive other types of magnetic sensors.

Besides the modulator, a modified StrongARM comparator was designed and employed in the wake-up receiver block (WURX), which is insensitive to metastability error, preventing the generation of fake wake–up data and wasting energy due to processing such data. The designed WSN is supplied by the internal energy harvesting based power management unit (EH-PMU), in which the harvested energy from RF sources is stored in a supercapacitor to power up the rest of the system.

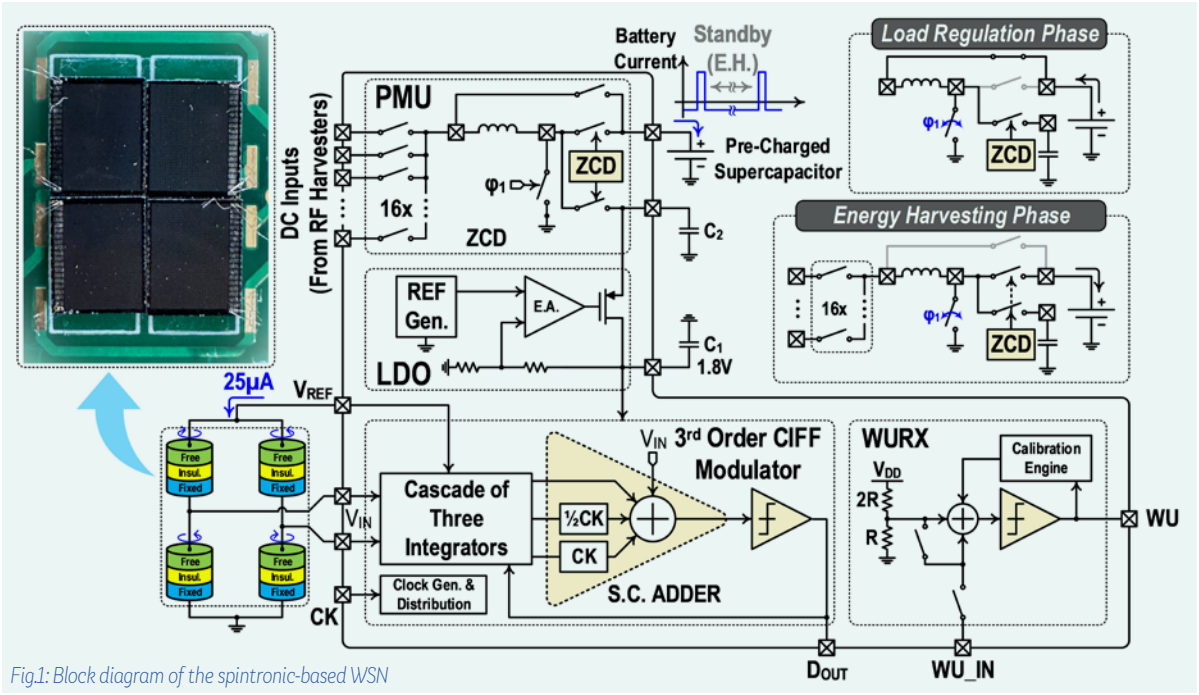

Fig.1: Block diagram of the spintronic-based WSN

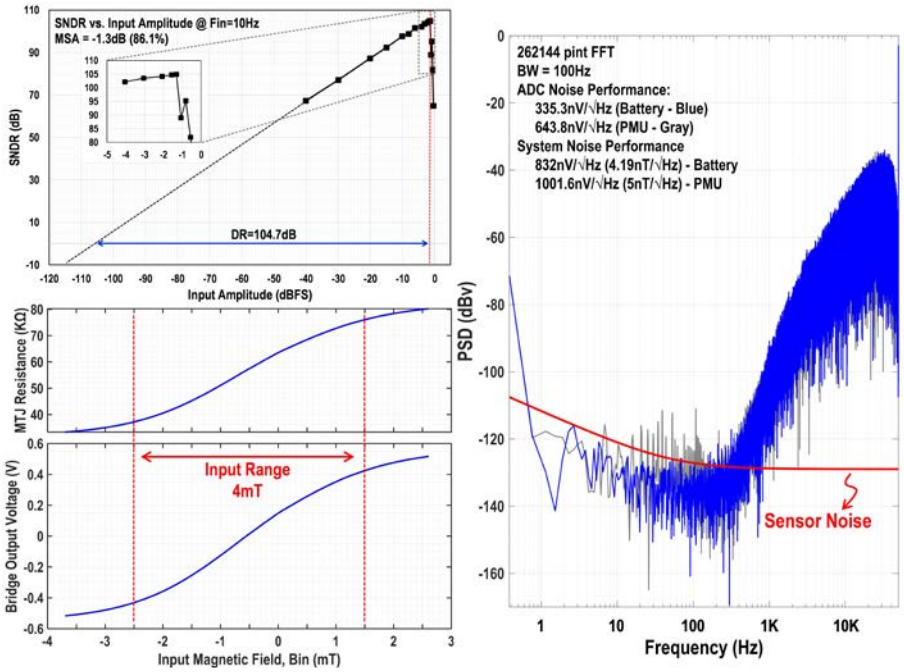

Fig.3: Measured input referred noise and DC characteristics of the DSM along with DC characteristics of the sensor bridge.

Since the required energy to supply the magnetometer is much higher than the typical harvested energy from RF sources, the operation of the EH-PMU is divided into two separate phases:

1. Harvesting Mode (HM): the input DC voltage generated by RF harvesters is boosted, and the corresponding energy is stored in the supercapacitor. Since the voltage conversion gain of the boost converter is always higher than 10 in this phase, the inductor is discharged much faster than its charging time, allowing the system to use the idle time of the PMU to harvest more energy from other input sources. In this design, 16 inputs were implemented to harvest energy from 16 sources operating in different frequency bands to enlarge the total harvested energy.
2. Backup Mode (BM): in this phase, the PMU is detached from input sources and connected to the supercapacitor to supply the magnetometer via the on-chip LDO with PSRR of 77dB at the PMU ripple frequency to avoid degrading the performance of the system due to supply ripple. Since the desired PMU should cover a wide range of the input voltage (from a few tens millivolts in HM to more than one volt in BM), a novel digital ZCD was designed that not only consumes less power than its analog counterparts but also benefits from digital design advantages without limiting the coverage range. The die micrograph of the fabricated prototype is shown in Figure 2.

Results

To test the system, the magnetometer was powered by a 1.8V supply voltage provided by the on-chip LDO connected to a 2.1V input voltage, consuming 213.6μW at 2.1V, in which the contribution of the MTJ bridge in the total power consumption is approximately 25%. Fig. 3 shows the measured noise performance of the readout circuit in both cases when the LDO is supplied by the internal PMU (gray) and when using a regulated voltage (blue), along with the PSD of the MTJ bridge. Measurement results show that the noise performance of 4.19nT/√Hz is achieved for the magnetometer, which is limited by the sensor noise. The measured DR of the DSM, along with the MTJ bridge characteristics, are also shown in Fig.3, indicating a DR of 93.6dB with an input range of -2.5/+1.5mT for the magnetometer.

The input offset of the comparator was successfully calibrated to the desired value (1mV), enabling the system to detect an input signal with an amplitude of 1.2mV while avoiding generating fake signals. Time domain measurement results along with the power consumption of the WURX are shown in this figure as well.

The inductor current of the PMU was measured using a current probe, along with the PMU output voltage and inductor voltage for three different input voltages in both HM and BM, showing that the proposed ZCD operates accurately across a wide input range (from 34mV to 1.25V). To evaluate the robustness of the proposed ZCD and the converter, the same measurements were performed on five different chips. The results show that the PMU achieves a peak efficiency of 86.5%, maintaining the reverse current below 8mA under all conditions.

The measured performance of the designed magnetometer and state-of-the-art works are summarized in Fig.4.

	ISSCC'24 Akita [1]	JSSC'22 Garcha [2]	ISSCC'15 Kashmiri [3]	ISSCC'07 Magnes [4]	ISSCC'07 Schott [5]	This Work
Sensor	MI	IFG	IFG	FG	Hall	**MTJ**
Technology	0.18µm	0.25µm	0.6µm	0.35µm	0.35µm	**0.18µm**
Output Type	Digital	Digital	Digital	Digital	Digital	**Digital**
Input Range	±80µT	±2.4mT	±1.32mT	±2µT	±0.5mT	**-2.5/+1.5mT**
Bandwidth	10KHz	125KHz	75KHz	30Hz	100Hz	**100Hz**
Noise	45pT/√Hz	500nT$_{rms}$	212nT$_{rms}$	3.3pT/√Hz[1]	244nT$_{rms}$[2]	**4.19nT/√Hz**
Dynamic Range	82dB	71dB	73dB	98dB	NA	**93.6dB**
Power	3.96mW	13mW	280mW	213mW	11mW	**213.6µW**
FOM[3]	1.25fW/Hz	4.51fW/Hz	96.3fW/Hz	580fW/Hz	26.2pW/Hz	**0.94fW/√Hz**
Size	5.71mm^2	7.6mm^2	9.8mm^2	20mm^2	6.4mm^2	**4.87+4 mm^2**

[1]Estimated from DR and input range [3]
[2]Estimated from resolution and input range
[3]FOM=Power/(BW x (input range / rms noise)^2)

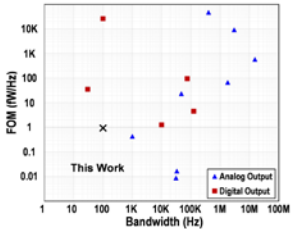

Fig.4: Performance summery table and comparison with state-of-the-art magnetometers

Compared to previous works, the described magnetometer has a wide input range and µW level power consumption, which is crucial for power-restricted applications. Although the BW of the system is lower than the other works (100Hz), the presented system exhibits the lowest FOM among all digital output magnetometers.

Why Europractice?

Using Europractice mini@sic service we were able to fabricate our design in a small area, thereby lowering the total cost of the project. Additionally, their support team provided us different feedback on our GDS file during a smooth back-and-forth process.

Acknowledgements

This work was supported by the SWAN-on-Chip project, funded by the European Union's Horizon 2021-CL4-2021-Digital-Emerging.

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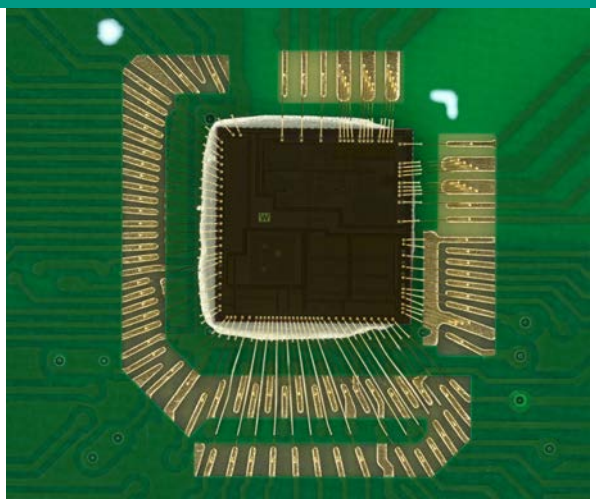

Fig.1: Picture of the wired chip on board.

CONAN: a radhard electronic circuit breaker

Weeroc, Villebon-sur-Yvette, France

Contacts: Julien Fleury, Jean-Baptiste Cizel, Cyrille Derrien, Salleh Ahmad, Stéphane Callier & Al
E-mail: julien.fleury@weeroc.com
Technology: X-FAB XT018
Die Size: 4000µm x 4000µm
Application Area: (Aero)Space

Introduction

Switching and protection function on satellite power lines are ensured today by fuse boxes. Having an electronic function handling in an agile way both switching and protection with many telemetry and telecommand features. ESA has opened an ARTES-AT, and Weeroc has answered the call together with Airbus Defence and Space for the end-user specification. CONAN chip is the successful outcome of that ARTES-AT.

Description

CONAN is a space-grade electronic circuit breaker and current limiter controller aiming at driving one or two PMOS (nominal

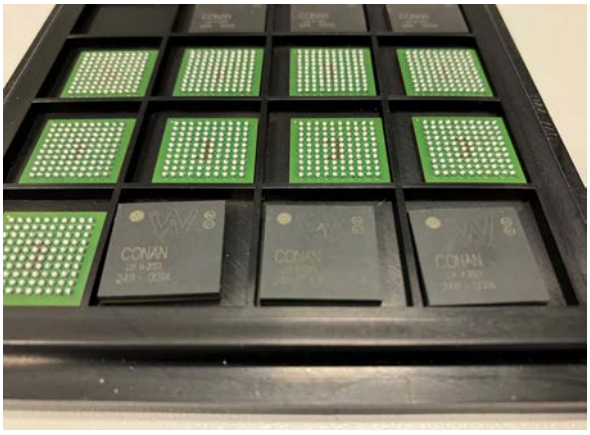

Fig.2: Picture of the packaged CONAN.

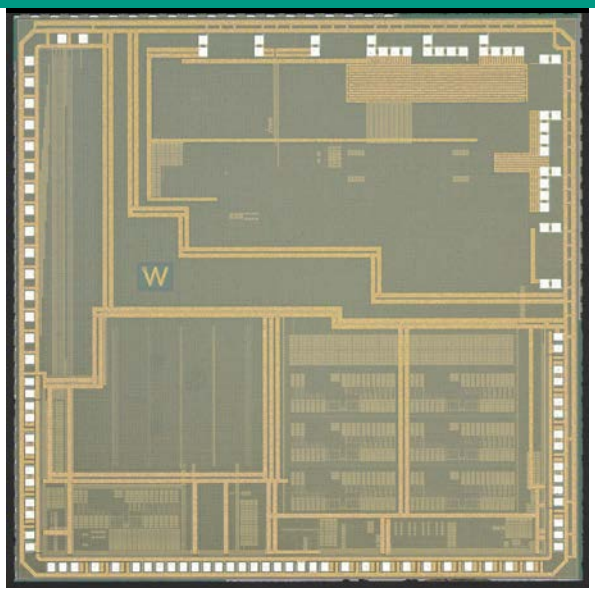

Fig.3: Picture of the naked die.

or nominal and redundant) to ensure programmable and fail-safe power control on rail from 20V to 130V with a current limitation up to 12A.

CONAN can be programmed to trip on UVD, excess temperature, over-current consumption and can either restart automatically or upon user request. The controller can be programmed through a dual serial space bus (nominal and redundant) or be used as a standalone device programmed by resistors.

CONAN acts as a current limiter with programmable threshold and trip time. Several parameters (power rail voltage, output voltage, redundant MOSFET voltage, current, temperature) are constantly acquired as telemetry parameters and can be sent by the serial bus.

CONAN can control 8 heaters using up to 15V internal drivers.

Results

CONAN has been tested in temperature and radiation and is compatible with space-grade missions. Telemetry and telecommand features have been successfully tested. Regulation and trip off are working nicely, and the chip is fully functional. Some parameters will be improved in the next version to be qualified for flight.

Why Europractice?

Europractice helped us by proposing an MPW allowing us reducing the cost of the first prototype. Europractice also managed the design kit for us during the technology change during the project.

Acknowledgements

Thanks for the support of ESA ARTES-AT program, CNES, and Airbus Defence and Space.

Quantum information with integrated photonics

National Institute for Nuclear Physics (INFN), Rome, Italy

Contact: Andrea Salamon
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Technology: CORNERSTONE Si-Photonics 220 nm SOI passives
Die Size: 5.5mm x 4.9mm
Application Area: Quantum Computing

Introduction

Quantum Information is the branch of Science and Technology dedicated to the exploitation of quantum phenomena for the processing and transmission of information [1]. Various technological platforms were proposed for this purpose and over the past years systems based e.g. on photons, superconducting devices, trapped ions, Rydberg atoms were developed [2].

In recent years, thanks to the progress of lithographic techniques, it has been possible to make significant progress towards integration of complex quantum functions on a single integrated photonic circuit [3,4].

Description

In recent years a project was funded by INFN, the Italian National Institute for Nuclear Physics, with the aim of developing integrated photonic quantum circuits and devices on a common Silicon on Insulator (SOI) platform.

Four research lines are currently being investigated in this project:

1. the design of silicon photonic circuits for Linear Optics Quantum Computing;
2. the engineering of integrated Single Photon Sources via emitter centers creation through controlled ion implantation [5];
3. the use of new classes of materials such as topological insulators for integrated Single Photon Detectors [6,7];
4. the use of nanomaterials such as graphene and semiconductor nanowires for Integrated Polarization Control Devices [8,9].

Results

A post selected probabilistic Controlled NOT for Linear Optical Quantum Computing in 220nm Silicon on Insulator technology

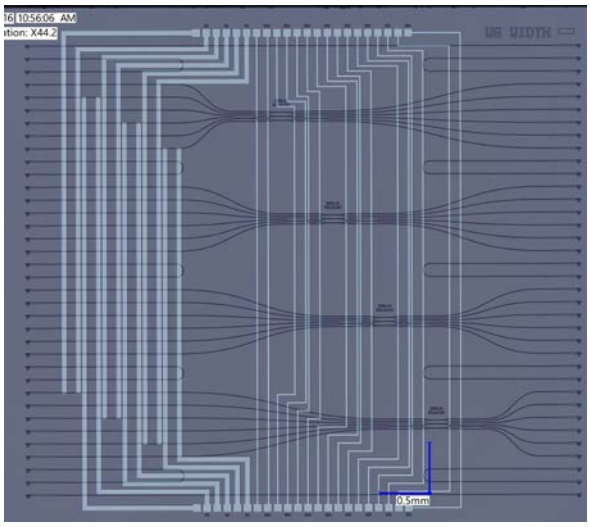

Fig.1: Microphotograph of the 220nm SOI post selected probabilistic Controlled NOT, produced at CORNERSTONE (5.5mm x 4.9mm).

was simulated, designed and produced at CORNERSTONE, see Figure 1.

The Controlled NOT Photonic ICs were wire-bonded on the test printed board (connected to dedicated current sources needed to drive the Photonic IC thermal phase shifters and glued to a Peltier cell for global thermal control) and coupled to custom designed fiber arrays. The tests performed so far (measurement of chip to fiber optical coupling, characterization of Controlled NOT directional couplers and thermo-optical phase shifters) are perfectly in line with simulation results.

The process of deterministic single ions implantation on silicon substrates was optimized and various colour centers activation techniques were studied. The possibility of depositing controlled layers of topological insulators (e.g. Bi2Se3) on small silicon areas for integrated photon detector implementation was demonstrated. Single nanowires, nanowire chains, and hexagonal boron nitride flakes were deposited on silicon waveguides and connected to metal tracks to allow light polarization control. Based on these preliminary tests a dedicated custom Photonic IC in 220 nm Silicon On Insulator technology was designed and sent to production at CORNERSTONE, see Figure 2.

Why Europractice?

Europractice allowed us to get affordable access to state of the state-of-the-art EDA tools and to avail of additional technical support and some extra discounts as a Europractice member on CORNERSTONE MPW runs.

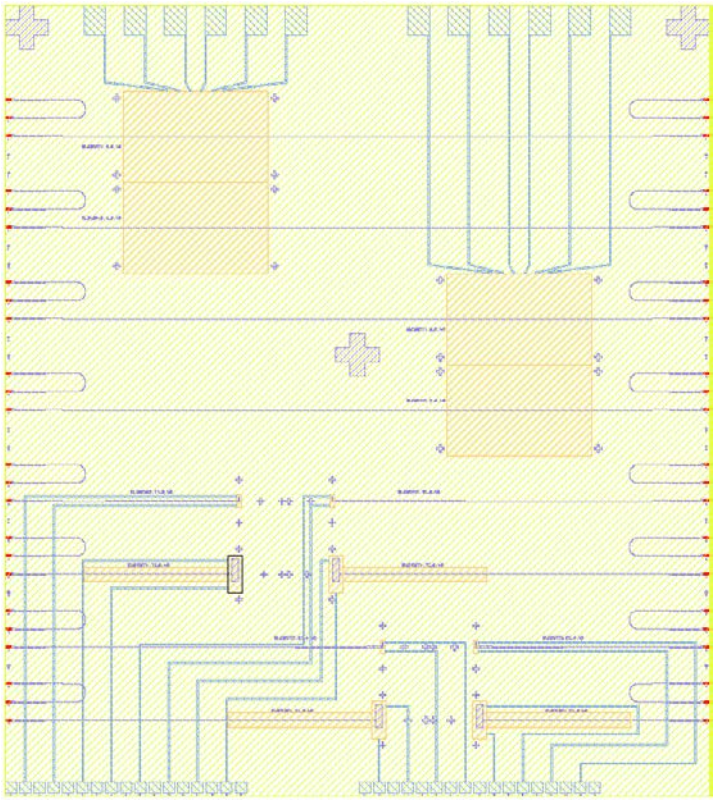

Fig.2: GDS of the 220 nm SOI Photonic IC for single photon sources, detectors and polarization control circuits sent to production at CORNERSTONE (5.5mm x 4.9mm).

Acknowledgements

This work was funded by INFN QUANTEP experiment and by PNRR MUR project PE0000023-NQSTI (Italy).

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Silicon Photonics for the optical readout of future CERN detectors

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Contacts:	Carmelo Scarcella, Jan Troska
E-mail:	jan.troska@cern.ch
Technology	imec Si-Photonics iSiPP50G
Die Size:	5.1mm x 5.1mm
Design Tools:	Synopsys OptoDesigner
Application Area:	High Energy Physics (HEP)

Introduction

Fibre optic links are essential in High Energy Physics (HEP) experiments, allowing the transmission of large volumes of data from particle detectors operating in harsh radiation environments, to radiation-free zones. Silicon Photonics (SiPh) has emerged as a promising technology for the next generation of optical readout systems for CERN detectors. Compared to the current generation of data links for CERN detectors, which are based on discrete optoelectronic components, Photonic Integrated Circuits (PICs) offer higher radiation tolerance, higher bandwidth, reduced power consumption, and lower mass.

Description

A PIC named SystemPIC was designed by CERN and fabricated using the imec iSiPP50G technology through a Europractice multi-project wafer (MPW) run. The test circuits integrated in the PIC utilise various mature building blocks from the Process Design Kit (PDK) provided by imec. Key components include waveguides, fiber couplers, high-speed ring modulators, and Germanium photodiodes. Additionally, we developed custom ring modulators with enhanced radiation tolerance and an optimised trade-off between efficiency and bandwidth, tailored specifically to our application. The target system is a four-channel Coarse Wavelength Division Multiplexing (CWDM) data link, where each µ-ring modulator operates at 25.6 Gb/s.

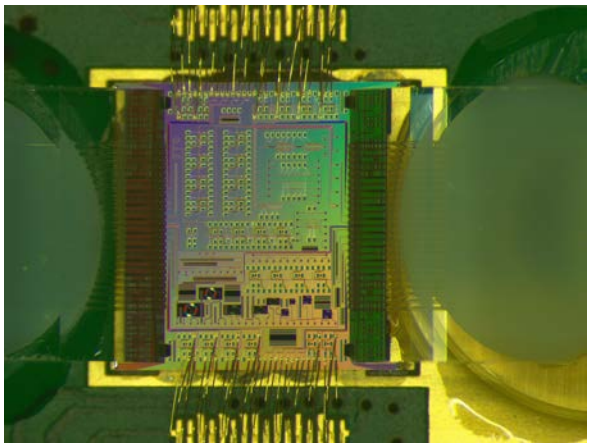

Fig.1: Micrograph of the fabricated SystemPIC wire-bonded onto a test board and pigtailed on both sides with 24-channel single-mode fiber arrays.

Results

The SystemPIC was first employed to evaluate the radiation tolerance of Silicon Photonics components. Figure 1 shows the SystemPIC wire-bonded to a test board and pigtailed on both sides using a 24-channel fiber array. The test board provides electrical and optical connection to 12 ring modulators and 8 photodiodes, allowing to measure the devices during the irradiation test. Results indicate only minor performance degradation up to relatively high radiation levels.

The SystemPIC was the test vehicle to validate the concept of co-packaging SiPh optical transceivers with particle sensors. Fig.2a and 2b show the SystemPIC assembled back-to-back

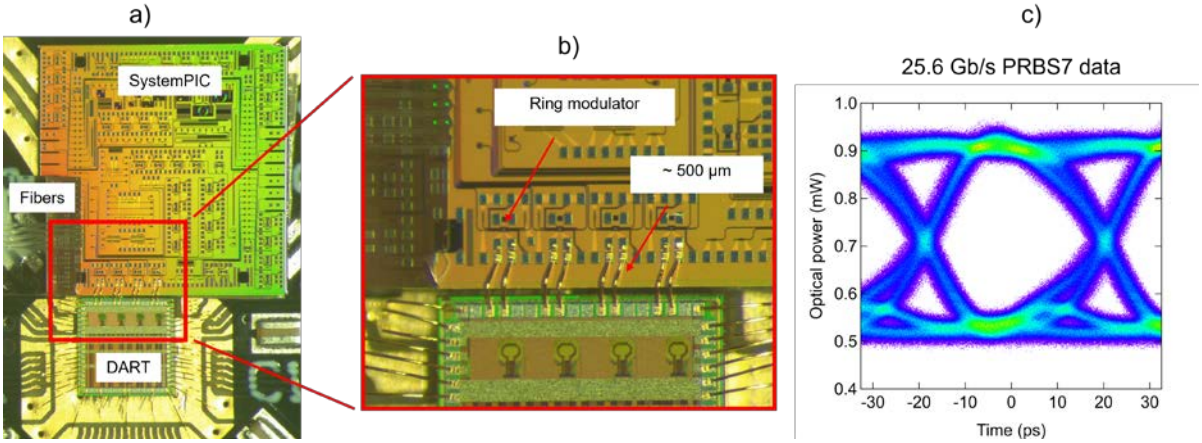

Fig.2: a) and b) Co-packaging of the SystemPIC with a CMOS custom quad modulator driver; c) A wide-open optical eye diagram was measured on this demonstrator.

with a 4-channel radiation-tolerant modulator driver fabricated in 28 nm CMOS technology (DART28). The PIC functions as an optical chiplet, located next to the high-speed outputs of the electronic ASIC. Fig.2c shows a wide optical eye diagram acquired from this demonstrator at 25.6 Gb/s, the target line rate for our project.

For the first time, we were able to benefit from the low coupling loss and the flat bandwidth of edge couplers, which is essential for CWDM modulation schemes. Figure 3 shows the SystemPIC pigtailed on both sides with 8-channel fibre arrays using the edge-coupling technique. The measured fiber-to-waveguide coupling loss was approximately 2 dB over the entire O-band. To match the small mode field diameter

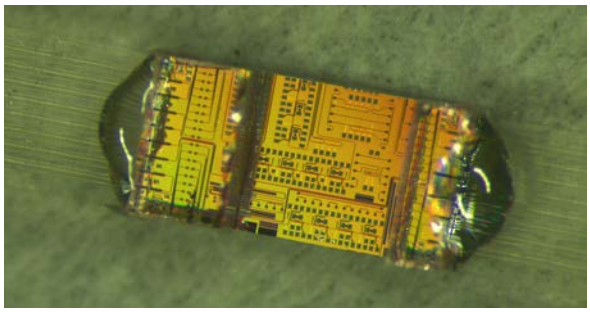

Fig.3: Picture of the first PIC pigtailed on both sides with 8-channel fibre arrays using the edge coupling technique.

(MFD) of the edge-couplers, we used an array of UHNA4 fibers. We are looking forward to the introduction of the Silicon Nitride process module, which will enable edge-couplers with an MFD compatible with standard single-mode fibers.

Why Europractice?

Europractice provides a unique opportunity for our R&D program by offering access to cutting edge Silicon Photonics fabrication processes through multi-project wafer runs. It also provides access to the necessary EDA software and valuable training on these design tools. Our team has already taped out 4 distinct PIC designs using the imec Silicon Photonics platform. We appreciate a solid support provided through the Europractice framework by imec and Synopsys at all stages of design and testing.

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Exploring IC Design and Wire Bonding with Pragmatic Technology: A Research Perspective

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Technology: Pragmatic Helvellyn FlexIC; wire-bonding at VTT
Die Size: 3mm x 3mm
Application Area: Education

Introduction

At Aalto University, our focus is on advancing research and innovation. This project represents our initial exploration of Pragmatic technology, aiming to evaluate its performance through the implementation of fundamental circuit blocks such as those included in this design. By analysing these blocks, we aim to gain valuable insights that will guide the integration of more complex systems in future SoC tape-outs. Pragmatic technology was chosen for its novel approach to flexible IC fabrication, providing a valuable platform for evaluating new methodologies in IC design.

Description

Prof. Halonen's group from Aalto univeristy has designed an integrated circuit (IC) utilizing the Pragmatic technology platform with the Helvellyn v2.1.0.beta.2 process design kit (PDK). The chip, measuring 3mm × 3mm, serves as an educational tool for both design exploration and performance evaluation. The IC incorporates two primary functional domains:

1. On-chip Circuit Blocks for a Sensor Node: This section includes a capacitance-to-frequency converter, a power management unit with regulation, and control circuitry interfaced through an SPI protocol.
2. Analog Computing Node: This area features key components such as a multiplying digital-to-analog converter (MDAC) and operational amplifiers.

VTT Technical Research Centre of Finland Ltd. performed the wire-bonding of the Flex IC. The Flex IC was glued onto a PCB with non-conductive adhesive. The handling of the thin chip required a great care. The wire-bonding tests were carried out by manual and automatic wedge & ball bonders. Both Al and Au

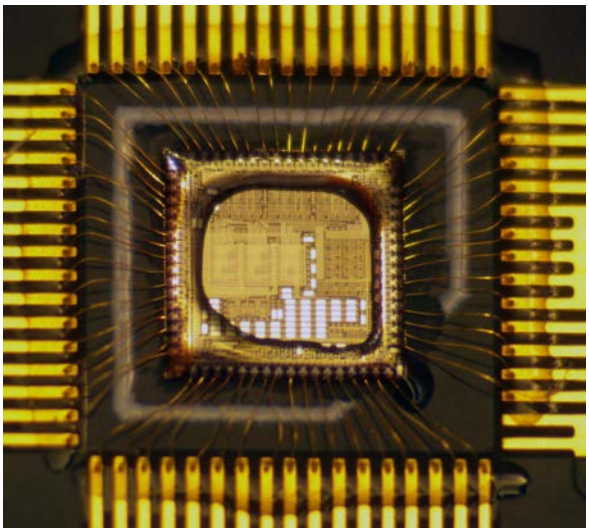

Fig.1: Top view of the FlexIC device illustrating wire-bonding connections across all pads.

wires were used, and eventually, 17.5µm Au wire was selected for most of the tests. The wire-bonding on ENIG-plated PCB worked well. It was found out that the bonding on Al pads on the chip was challenging. However, by optimising the bonding parameters with the automatic ball bonder it was possible to make wire-bondings. Eventually, the bonding joints were protected using encapsulation adhesive, which was UV-cured. Figure 1 shows the wire-bonded ASIC.

Results

The devices are currently undergoing testing. However, several of the fabricated devices on this chip have already been published, along with post-layout results. The references to these publications are listed below.

Why Europractice?

At the ELEC Department of Aalto University, we have been leveraging the services of Europractice for ASIC fabrication for many years. The platform has consistently provided us with access to advanced technologies, reliable support, and an efficient pathway to realise our designs. This longstanding relationship has greatly benefited our research and educational initiatives.

For this specific project, we utilised Pragmatic technology for the first time through Europractice. While there was some delay in the process, it is understandable given that the technology is relatively new and still maturing. The Europractice team provided us with valuable guidance throughout the process, ensuring that we could successfully navigate any challenges and meet our objectives.

Overall, our experience with Europractice remains positive. Their services continue to be an essential enabler for academic research and innovation in IC design, and we look forward to further collaborations in the future.

Acknowledgements

This work is supported by the Academy of Finland projects BL-SPIN (grant 13364029).

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Publications related to the design:

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PiezoMEMS transducers

CNRS – TIMA, Grenoble, France

Contact: Martial Defoort
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Technology: Science PiezoMEMS
Die Size: 11.15mm x 11.15mm
Application Area: IoT

Introduction

The physics of MicroElectroMechanical Systems (MEMS) has been studied for over a few decades and is nowadays present in most current technologies, in smartphones, cars, drones, IoT, and more. However, these systems may bring much more than what they are traditionally used for. In particular, driving these mechanical devices at large displacement leads to nonlinear behaviors, which complexity is often discarded for industrial purposes, but could actually create new, disruptive applications.

Description

To study nonlinear physics in mechanical structures, one first step consists in creating "model systems" which, by construction, behave like text-book equations and are therefore simpler to study.

Thanks to the piezoelectric layer made available by Science, the designed devices are convenient to use through linear piezoelectric transduction, so that nonlinear behavior only arises from the mechanical system itself. The chip was divided into four subdices, two of them dedicated for model systems applications. On the one hand, regular doubly-clamped beams of various lengths will enable to study string-like behaviors over a broad frequency range, from kHz to MHz. On the other hand, circular membranes of various diameters will make the bridge between such model systems and actual nonlinear-based applications, such as nonlinear Piezoelectric Micromachined Ultrasonic Transducers (PMUTs).

Results

First experimental results are yet to come, but it is expected that these MEMS will enable to gain more insight on how to exploit nonlinear physics for MEMS applications, from transducers to postprocessing units. In particular, such complex behaviors will open the paths towards more precise sensors and add functionalities such as random numbers generation [1] with very limited constrains.

Why Europractice?

Thanks to the CIME-P of Grenoble, France, and their Multi-Project Wafer solution, the use of Europractice Services has been very straightforward and convenient, enabling easy and fast access to actual devices.

Acknowledgements

This project was financially supported by the IRGA grant under the project SETH.

References

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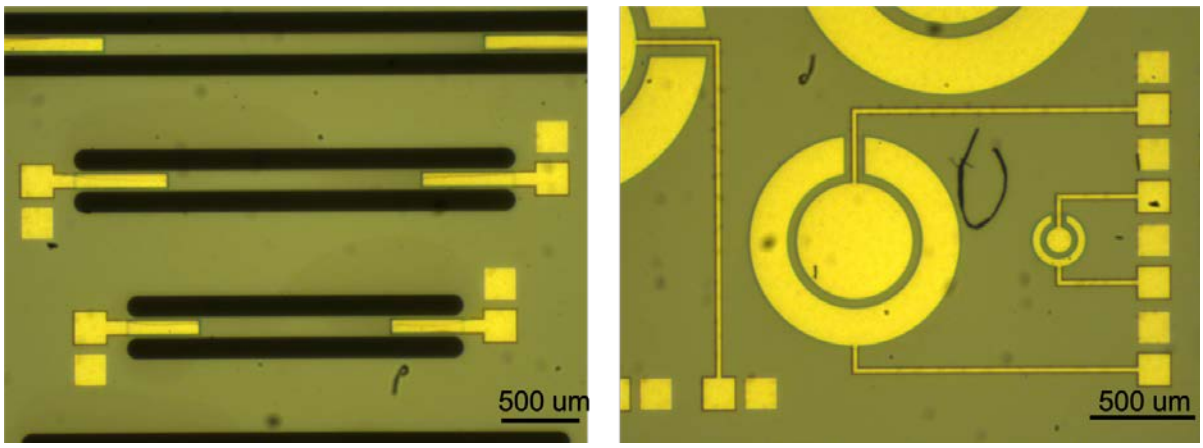

Fig.1: Optical photography of piezoelectrically actuated and sensed MEMS with (left) doubly-clamped beams and (right) circular membranes of various lengths and diameters.

56Gb/s Silicon Photonic Transceiver for Space

Mbryonics Ltd., Galway, Ireland

Contact: Alan Naughton
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Technology: System Integration
Application Area: (Aero)Space

Introduction

Mbryonics Ltd is an Irish SME with a key focus on the development of laser communications system for the satellite market. This includes both external links (optical intersatellite links, optical feeder links and optical downlinks) and intra-satellite links where there is a key focus on the use of optical transceivers for high-speed serial links linking digital payloads on board satellites. The SWaP advantages along with performance improvements possible using optical interconnects is now of great interest in particular for the emerging satellite constellation market. The transceiver being developed in this work is targeting this market with a key focus on reduced power consumption, radiation tolerance and high data rate with a co-packaged optics form factor the ultimate goal. This first prototype is a key step towards this goal.

Description

The device which was packaged through this activity is a 56Gb/s silicon radiation hardened photonic transceiver demonstrator targeting the space market. This is the first prototype in the development of Mbryonics' 56Gb/s co-packaged photonic transceiver for on-board optical links in satellite digital payloads.

Fig.2: 56Gbs silicon photonic transceiver system for space comminications.

Due to the high data rate being targeted the electrical integration was a critical step with flip-chip integration chosen to achieve the best performance. Work completed included: Flip-chip integration of multiple dies, Tx & Rx PICs, TIA, driver IC onto a common PCB and optical coupling of fiber arrays. EICs had 60um copper pillars and consist vertically of 45um Cu + 20 um SnAg.

Results

The packaging of the device has been sucesfully completed and it is still undergoing the final test campaign.

Why Europractice?

We have used Europractice services as they offered access to state of the art system integration processes and die level integration on low volume prototype developments. The service offered though this engagement was excellent and an overall very positive experience.

Acknowledgements

This work has been funded by the European Space Agency under Contract No. 40001305314000/20/NL/AR

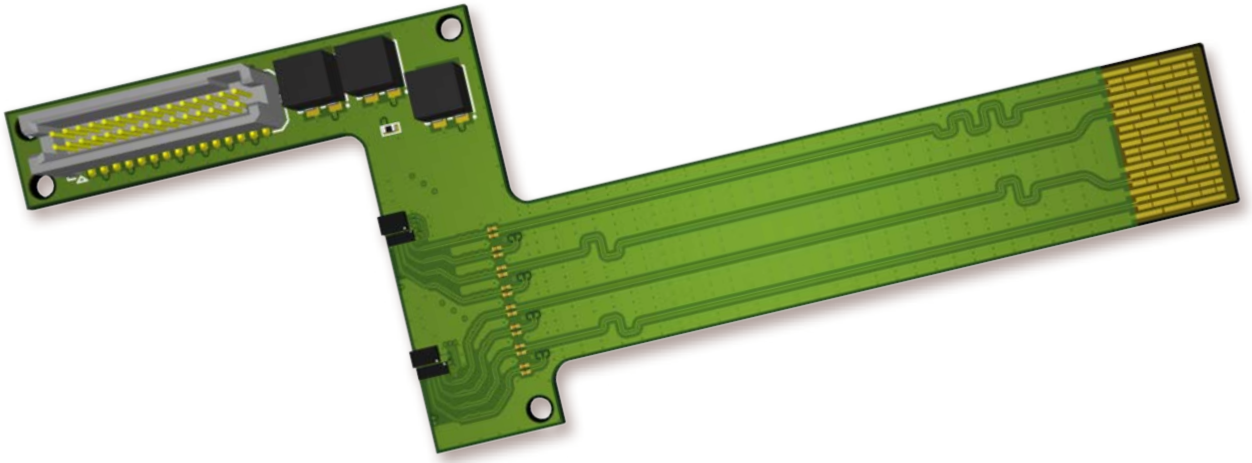

Fig.1: Multiple EIC & PICs flip-chip integrated onto a common PCB.

INTUITIVE: A Spike-based Per-Taxel Tactile Sensor Readout Chip with Integrated PVDF Sensors for Electronic Skins

MICAS, Department of Electrical Engineering (ESAT), KU Leuven, Leuven, Belgium

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Technology: Full-wafer run in TSMC 0.18µm CMOS (executed in 2022)
Die Size: 5.6mm x 3.8mm
Design Tools: Cadence Virtuoso, Cadence Spectre, Cadence Innovus, Siemens Calibre, Synopsys Design Vision
Application Area: Medical / Health

Introduction

High-resolution tactile sensing[1] is crucial for mimicking human behavior in robotic and prosthetic applications. This type of sensing is referred to as "electronic skin" (e-skin) and is made up of a network of sensors that measure parameters like force and shear. A promising approach is the use of neuromorphic tactile sensors [2][3] with end-to-end on-chip sensor-to-spike encoding performed at the hardware level.

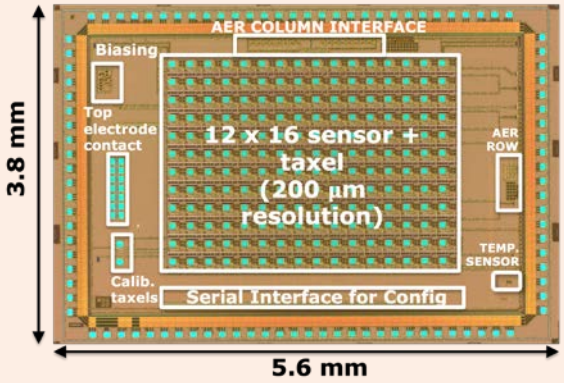

Fig.1: INTUITIVE chip micrograph (before sensor deposition).

While previous work on e-skin systems focused on large-area, low-spatial-resolution (>1mm) tactile sensing, this work mimics the fine-resolution sensing strategy in the human fingertips. To achieve that, it is necessary to achieve in silicon the same power-efficient and high-spatial-resolution sensing and local processing as in the fingertips.

We have integrated a dense tactile sensor array on a custom CMOS readout chip, allowing for dense and power-efficient readout with local processing capabilities. The sensor-to-readout chip integration supports dense per-taxel connections, enabling true per-taxel sparse-sampling conversion (i.e., spikes) as performed in human afferents, while also eliminating the

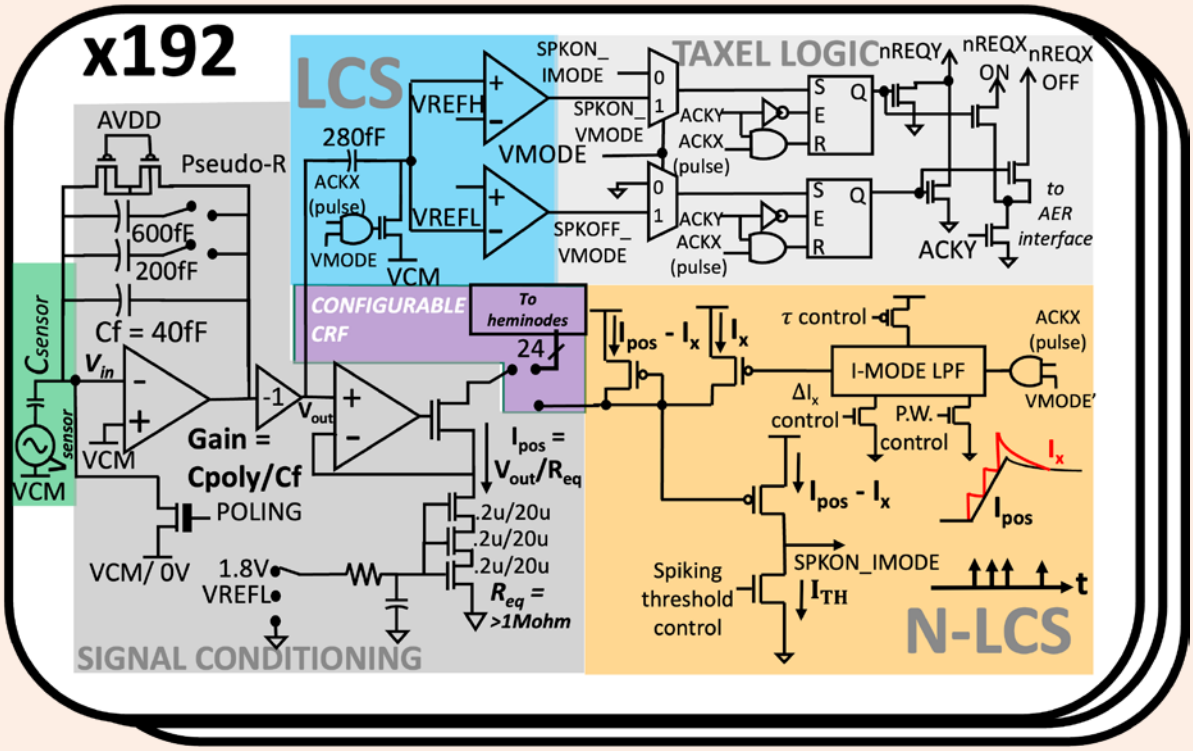

Fig.2: The per-taxel circuit architecture features signal conditioning and spiking readout channels. Output spikes are transmitted via an on-chip Asynchronous Event Representation (AER) interface.

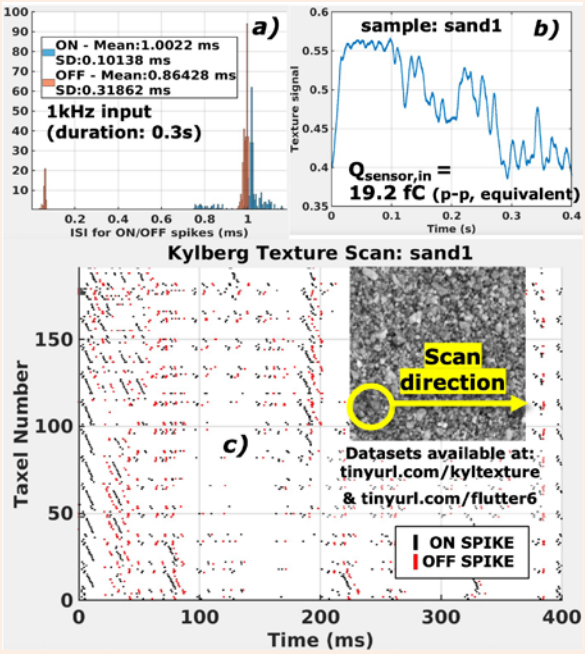

Fig.3: Measurement results: a) Inter-spike interval (ISI) (1 spike/period). b) Texture signal after the signal conditioning stage (estimated sensor capacitance=172 fF). c) Output spikes during an emulated texture scan.

mechanically-fragile sensor-to-readout wiring. For such sensor integration, polyvinylidene fluoride (PVDF)-based piezoelectric sensors deposited on top of the chip, offer a promising route due to their relatively simple structure and their CMOS-compatible fine lithography-based integration.

Description

The INTUITIVE chip, shown in Fig.1, features 12x16 taxels with two spiking readout channels each (Fig.2: a voltage-mode level crossing sampling (LCS), and a neuromorphic current-mode LCS converter. The dual readout channel design allows for flexibility in the spike generation depending on the application (robotics, neuroprosthetics, etc.). The LCS channel detects signal changes and generates bipolar spikes through two window comparators while the N-LCS outputs unipolar spikes through a delta-modulator. In the N-LCS, its output spikes are integrated through two current-mode low-pass filters (fast and slow time constant), forming an exponentially decaying threshold for spiking and mimicking biological neuron spike encoding.

After wafer planarization, a PVDF solution of PVDF-TrFE (Piezotech FC20) is spin-coated on a 22.5 x 24 mm reticle cut of the wafer to integrate a 250µm sensor layer. This post-processing step was performed at Fondazione Bruno Kessler, Italy.

Results

This work is the first demonstration of on-chip end-to-end e-skin sensor-to-spike encoding with embedded CRF processing at fingertip-mimicking high taxel density. Compared to prior texture-sensing e-skins, this work achieves around 100-7000× reduction in the system power consumption and >5 orders of magnitude reduction in the per-taxel power consumption, while enhancing the spatial resolution by 5× to 200µm, and doubling the sensor count.

Figures 3(a)&(b) present the measured inter-spike interval (ISI) and the texture signal after signal conditioning, respectively. The tactile stimuli classification using the chip's output spikes (Fig. 3(c)) is performed off-chip by training a 256-LIF neuron, 1-hidden layer SNN network with Surrogate Gradient backpropagation, then fitting a Linear SVM classifier on the average spiking rate of the trained SNN's hidden layer. This method achieves a classification accuracy (across 6 k-folds) of 97.1% on the Kylberg texture dataset and of 99.2% on the flutter (0.5-15Hz) dataset.

Why Europractice?

The integration of the PVDF sensor, implemented as a post-processing step, necessitates large reticle areas, leading to the decision to procure wafers rather than individual dies. Europractice has been highly supportive in accommodating this request, offering prompt and valuable technical guidance throughout the design and fabrication stages.

Acknowledgements

This project has been funded in part by the European Union's Horizon 2020 research and innovation programme under the Marie Sklodowska-Curie grant agreement No 861166 (INTUITIVE) and the KU Leuven C3 Project DERMIS (Dense Electronic Readout for Multi-Scale Integrated e-Skin).

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[2] M. D. Alea, A. Safa, F. Giacomozzi, A. Adami, I. R. Temel, L. Lorenzelli, and G. Gielen, "A Fingertip-Mimicking 12×16 200µm-Resolution e-skin Taxel Readout Chip with per-Taxel Spiking Readout and Embedded Receptive Field Processing," 2023 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits), Kyoto, Japan, 2023, pp. 1-2, doi: 10.23919/VLSITechnologyandCir57934.2023.10185346.

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nanoSoC with custom accelerators for AI/ML

SoC Labs community – University of Southampton, UK

Contact:	Daniel Newbrook
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Technology:	TSMC 65nm (mini@sic)
Die Size:	1mm x 1.5mm
Design Tools:	Cadence, Synopsys
Application Area:	Education

Introduction

SoC Labs is a global community of academic researchers innovating in System On Chip ("SoC") design using Arm-based computing architectures. Our aims are to simplify SoC design in academic settings by supporting reusable SoC reference designs and IP. This enables academics to focus on their research/education and enables an easy path to proven silicon. The nanoSoC reference design is an entry-level reference design, ideal for small academic projects by PhD or other students to evaluate research hardware such as custom accelerators or signal processing subsystems with a low cost of fabrication, easy-to-adopt workflow and suite of verification assets and firmware.

Our aim is to help make SoC design and ASIC fabrication of those designs accessible for the 6000+ academic institutions worldwide.

Description

The nanoSoC reference design is a simple Arm Cortex M0 microcontroller SoC that can be easily extended to add custom subsystems. SoC Labs fabricated two separate ASICs using the nanoSoC reference design on a TSMC 65nm mini@sic shuttle. The two ASICs were the same core SoC, one with a Master's student-developed Systolic array AI/ML accelerator, and one with a PhD student-developed classifier for accelerated inference. The two SoC designs also used different DMA engines to drive their respective custom accelerators. The rest of the SoC system infrastructure was the same.

The use of the nanoSoC reference design allowed the two students at different academic institutions to use common design workflows and even the same test board for bringing up the manufactured silicon.

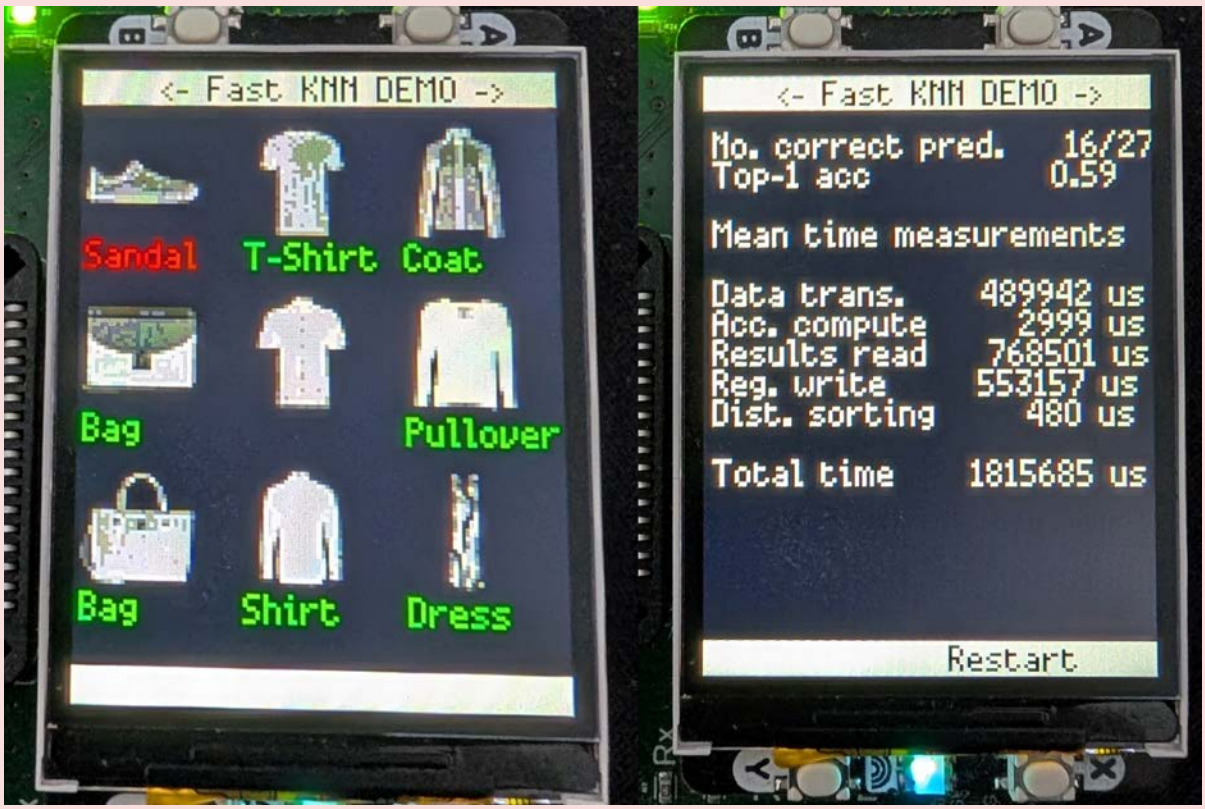

Fig.1: The output screen of the nanoSOC test board showing results from the FastKnn custom accelerator.

Results

The nanoSoC reference design has been demonstrated to provide all the necessary infrastructure to provide the early-stage PhD or Master's students with a solid grounding in the concepts of System on Chip design through to ASIC fabrication in an easily understood and adoptable form. Two novice students were able to undertake a complete SoC design, including their custom hardware and tape out, with a few months of effort.

As well as simplifying silicon implementations, the aim of the nanoSoC test board is to simplify the capture of statistics about the custom hardware design instantiated within the SoC by the students. PhD student Epifanios Baikas demonstrated his Fast-kNN classification hardware accelerator, which took 3.5 milliseconds to process a sample versus 10,500 milliseconds, using software on the nanoSoC Arm Cortex M0 core.

The nanoSoC utilises two power domains, one for the core system, and one for the custom subsystem. This allowed the students to measure the power of their accelerator designs separately from the system power.

The nanoSoC was implemented with a clock frequency of 240 MHz to allow an easy multiple of the max clock frequency of the I/O interface chip used on the silicon bring up test board.

Why Europractice?

SoC Labs is hosted at the University of Southampton, and we have many years of working with Europractice, taping out annually on the TSMC 65nm CMOS LP MS/RF (mini@sic) service and less regularly at more advanced nodes. Southampton have always found Europractice to be very responsive and supportive of our efforts to tape out.

We would like to work more closely with Europractice to help expand the reach of ASIC fabrication into more academic institutions. We believe that developing easily adoptable SoC reference designs, design patterns, IP, and especially verification assets, as well as creating opportunities to form hardware design communities across institutions to share expertise and support, will accelerate adoption.

Acknowledgements

SoC Labs acknowledges the support of Arm Limited for provision of the free to use Arm IP made available via the Arm Academic Access programme and their support of the SoC Labs community.

References

IEEE SOCC 2024, Special Session - SoC Labs, academic community SoC design using the ARM ecosystem, "Expanding diversity of SoC design in academia" by Epifanios Baikas, University of Southampton.

EUROPRACTICE MEMBERSHIP

Together with the funding provided by the European Commission, Europractice needs additional support to provide high quality service to more than 600 European universities and research institutes. Membership Fees pay for extra staff supporting this requested stimulation activity for academic institutions (not fully paid by the EC). The annual Membership Fee is collected by STFC on behalf of the Europractice project partners.

European universities and research institutes can choose from 4 different levels of membership:

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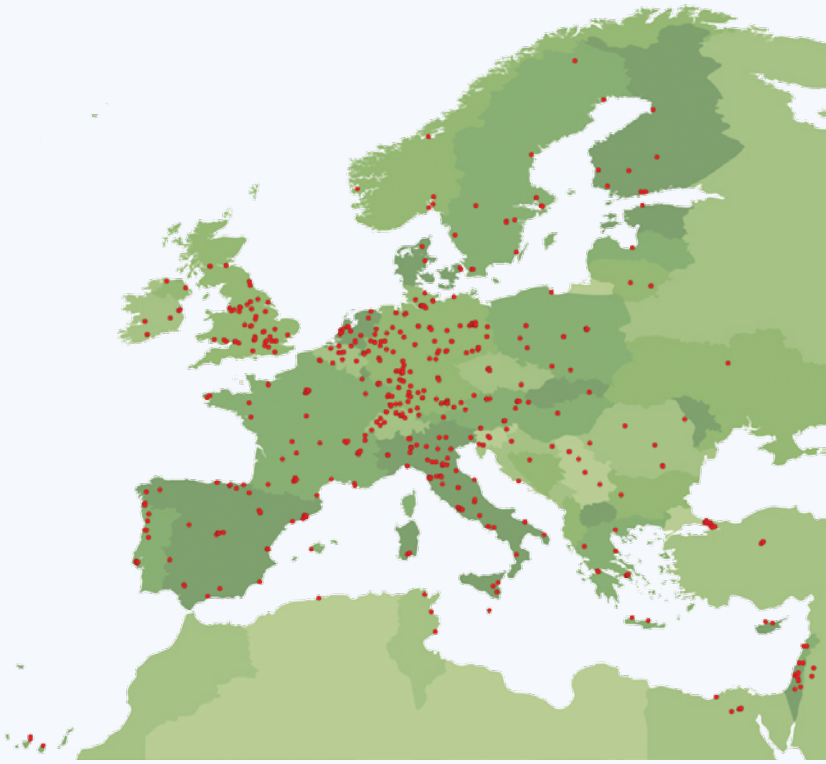
The number of academic members consists of more than 600 institutes in more than 40 countries from the EMEA zone (Europe, Middle East and Africa).



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